奈米技術在Flash記憶體與TFT平面顯示器之應用與研究

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奈米點(nano-dots)在半導體記憶體之製作與研究

Outline

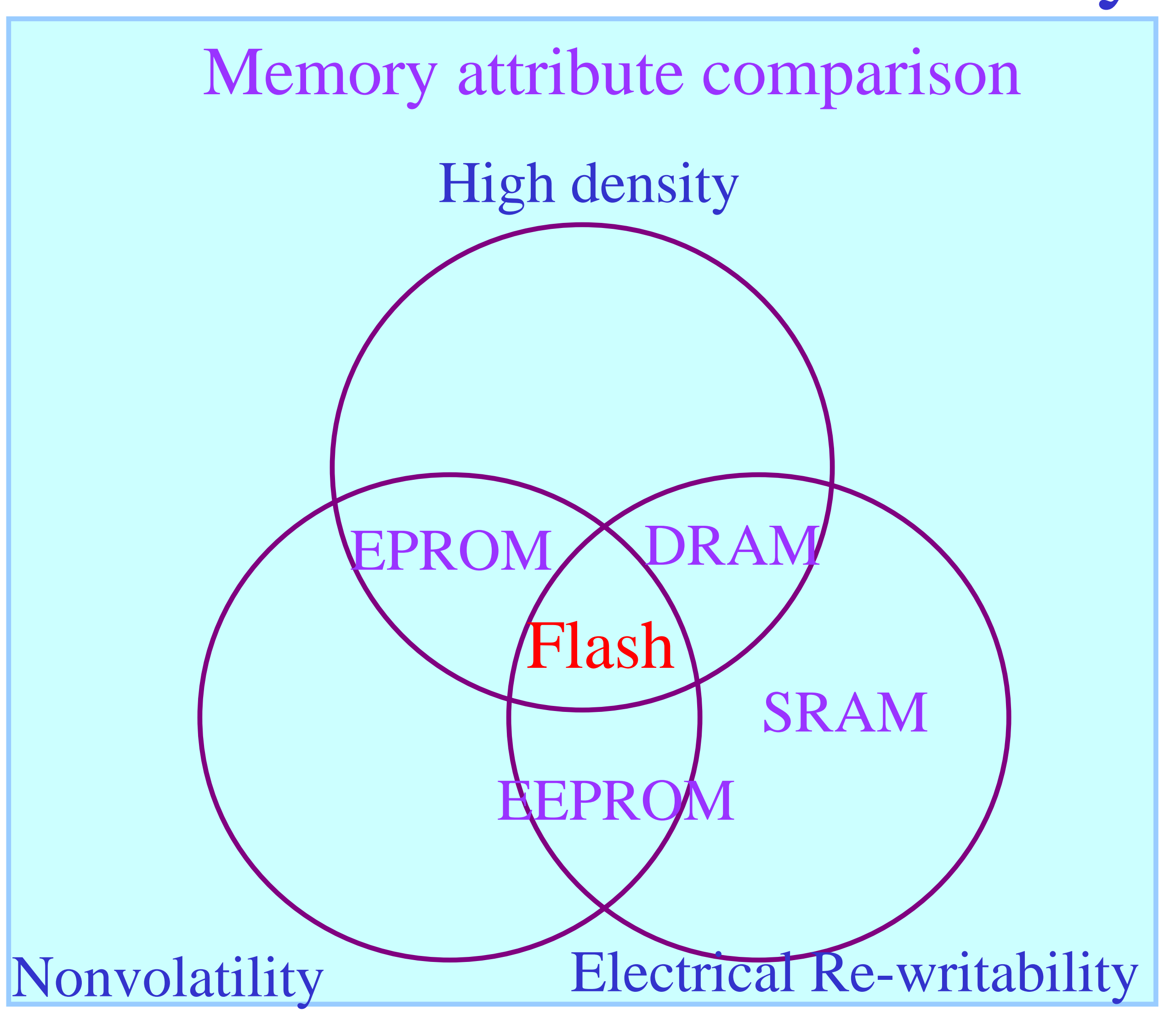
1. **Ge nano-dots** 在快閃記憶體之製作與研究

2. **GeO_2 nano-dots** 在快閃記憶體之製作與研究

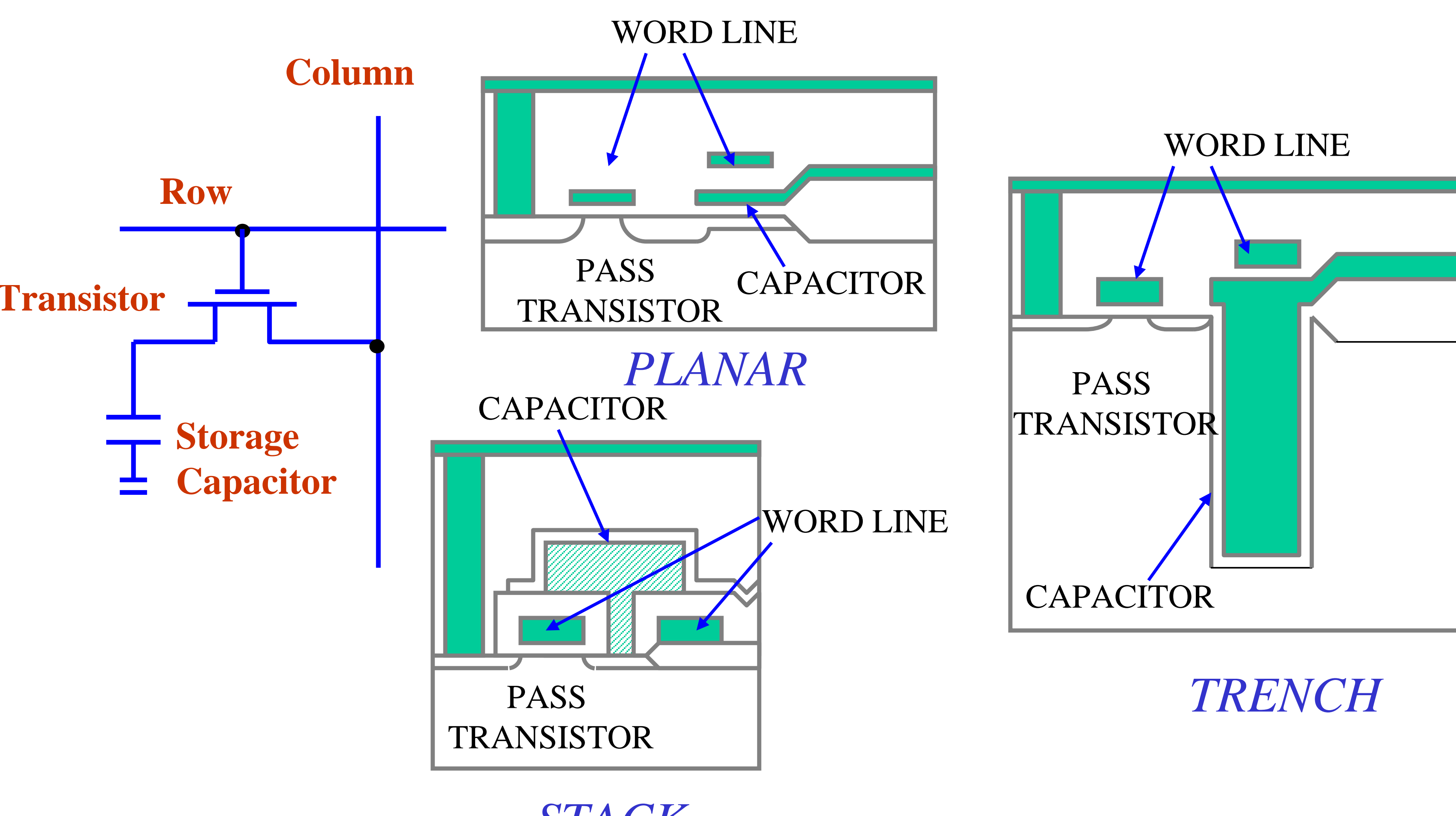
3. **W nano-dots** 在快閃記憶體之製作與研究

4. **SONOS** 非揮發性記憶體之製作與研究

Candidates of Ideal Memory

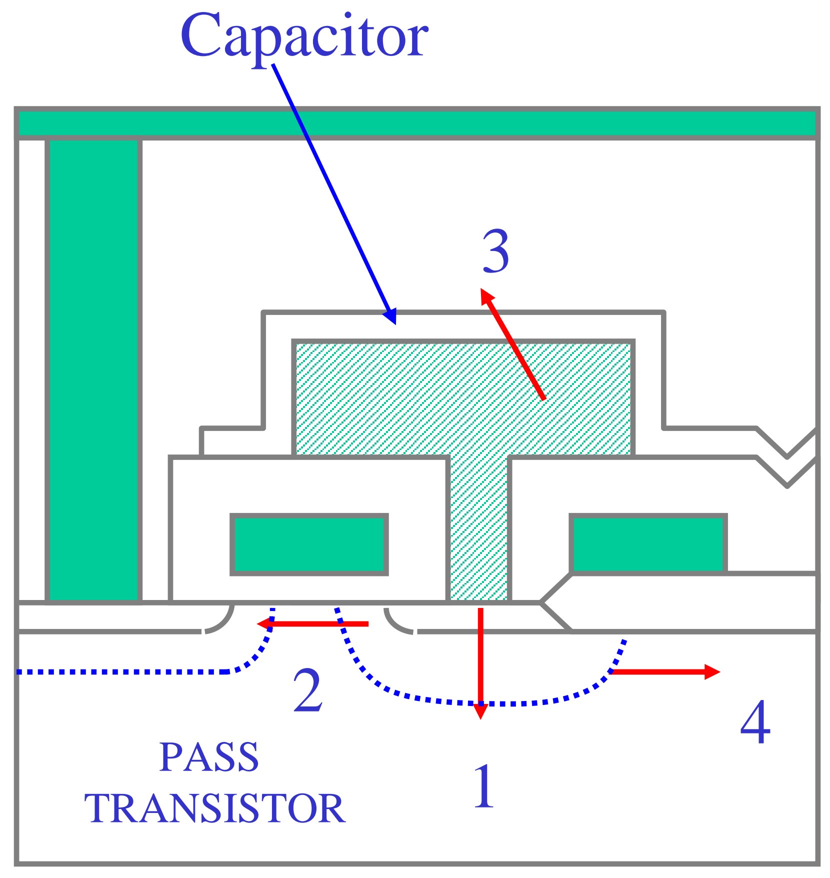


DRAM Cell Structure



Refresh

- Junction leakage
- Pass transistor subthreshold leakage
- Leakage through capacitor dielectric
- Other parasitic leakage paths

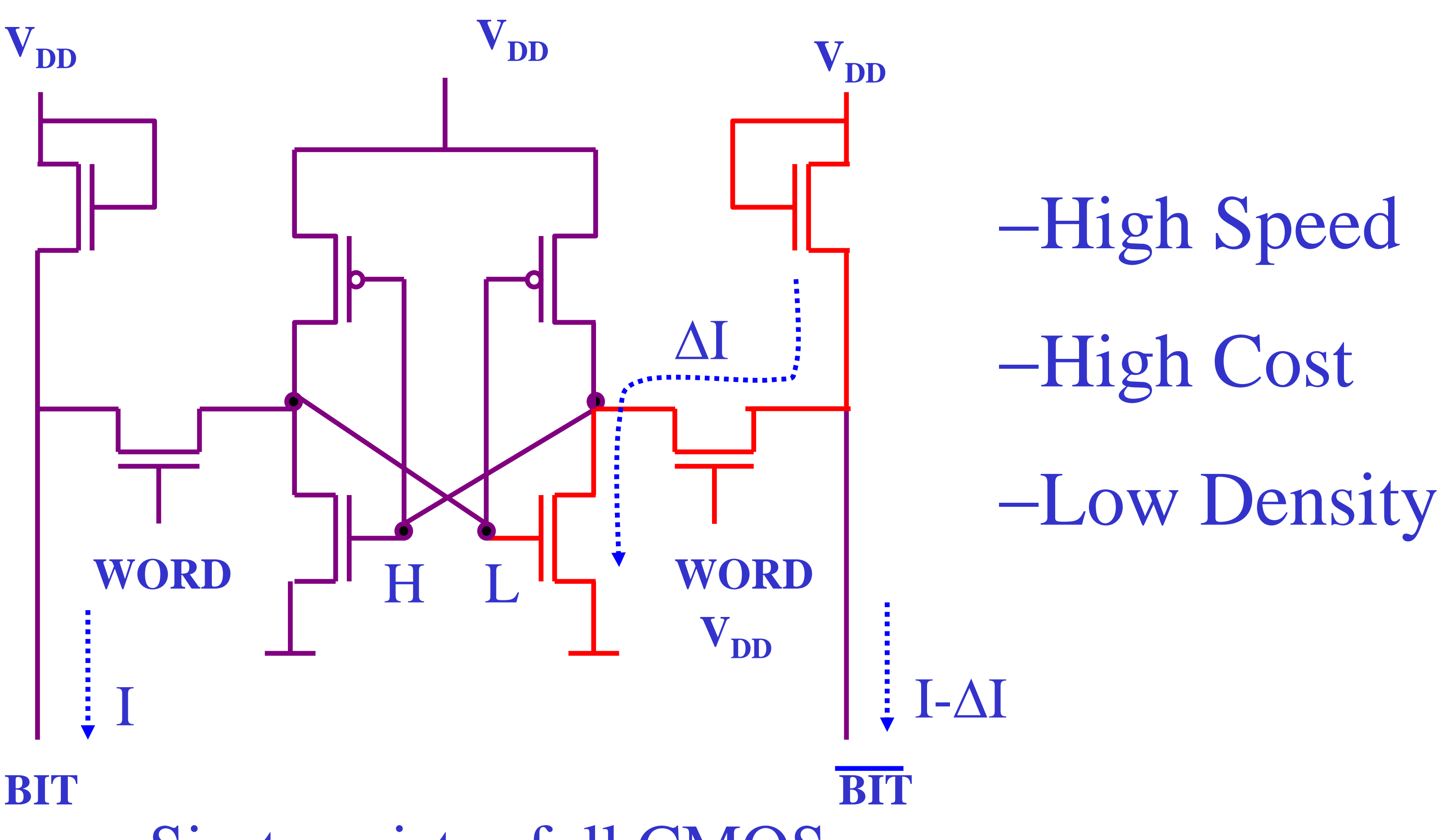


DRAM

- Disadvantages
  - volatile
  - low speed
  - power consumption (replenishing)
- Advantages
  - high density
  - low cost

DRAM still have the highest volume of memory market !!

SRAM



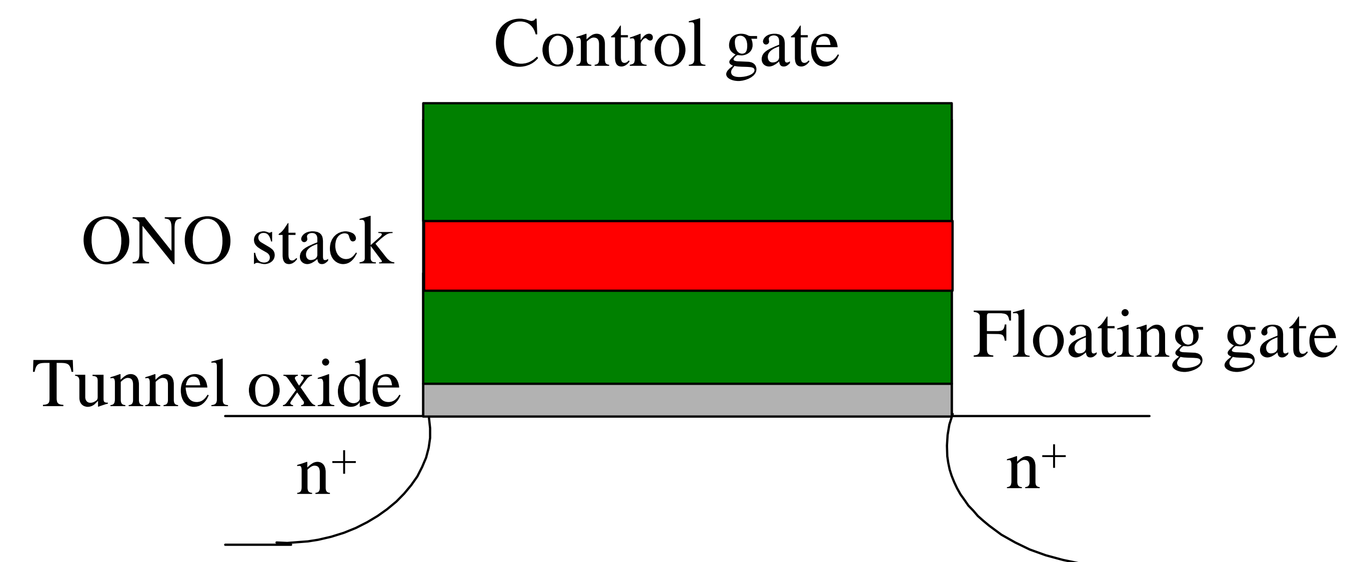
Six-transistor full CMOS

SRAM

- Mainly used as Cache
- SRAM are a quarter the capacity of DRAMs fro the same process technology and chip size

Cost about four times as much per bit as a DRAM!

Commercially successful floating-gate (FG) nonvolatile memory device



A substantial progress of NVSM - **portable electronic systems**

- Cell phone
- Laptop
- Digital camera
- Smart IC card
- Mp3 player
- ……..

- All of the devices require low power loss and being nonvolatile.

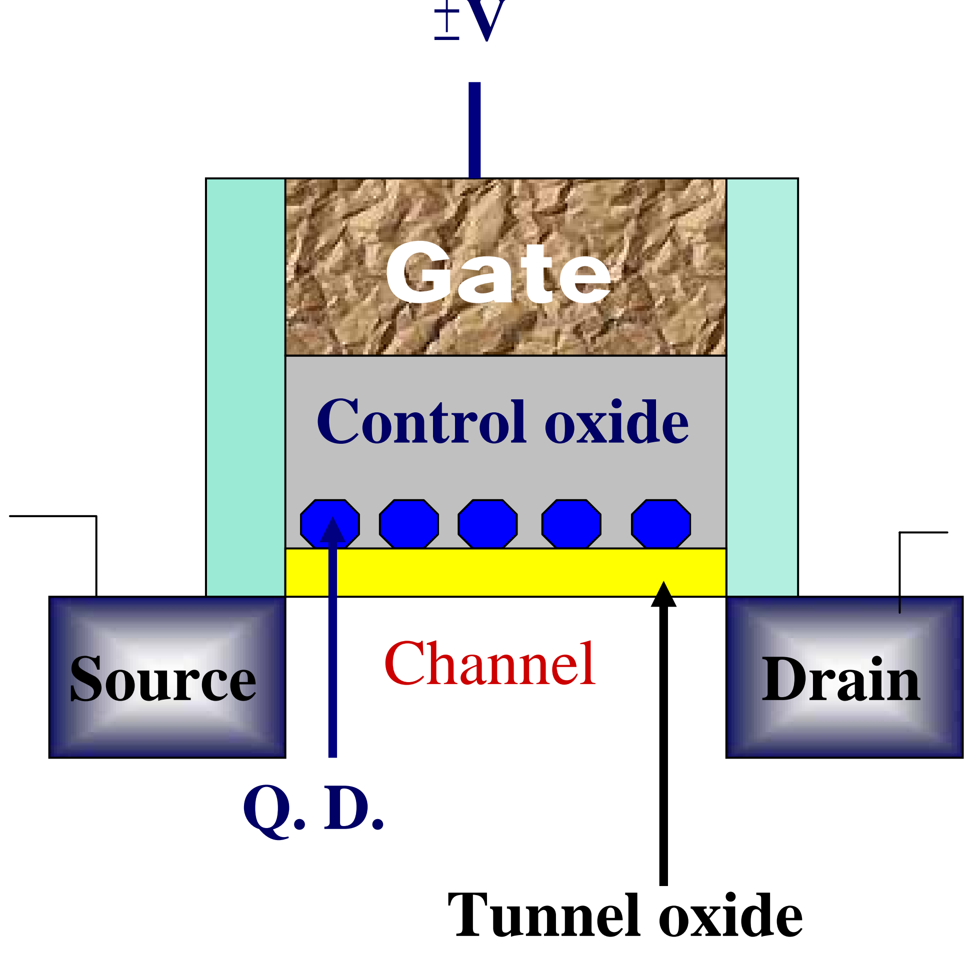
Web-Feet Research Inc.

Applications (M units)	2003	2004	2005	2006	2007	2008	2009	2010
Cellular	447	522	631	695	737	787	852	906
Bluetooth	37	61	85	163	194	212	234	251
Digital Cameras	59	78	85	105	116	125	131	139
MP3 Music Players	13	24	44	74	105	147	197	251
USB Drives	33	56	100	149	189	242	338	408
GPS (Auto, Marine, Aviation)	55	71	86	98	120	139	161	186
End-Use Total (M units)	2200	3131	3623	4091	4513	4930	5142	5568

Limitations of FG devices

- A compromise of 7-9 nm for tunnel oxide (low operating voltage v.s. high nonvolatility)
- One weak spot creates a fatal discharge path, compromising long term nonvolatility.
- Limitations for continued scaling.
- The FG structure is believed to run out of the steam beyond the 65-nm node.

Distributed Charge Storage -The introduction of nanocrystal (NC) memory device

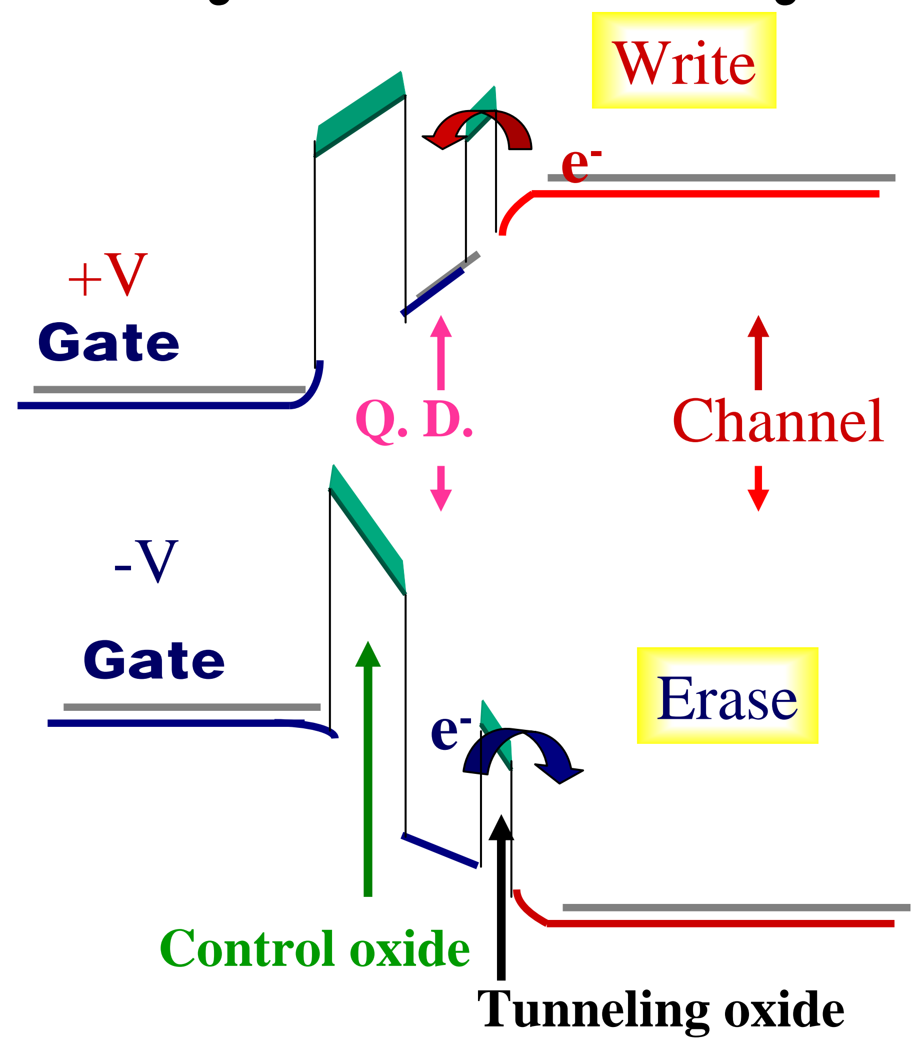


Distributed Charge Storage

- More simplified fabrication process
- The potential to use thinner tunnel oxide without sacrificing nonvolatility.
- Immunity to SILC, better retention and endurance characteristics.
- Great potential in device performance

→ **Write/Erase speed**

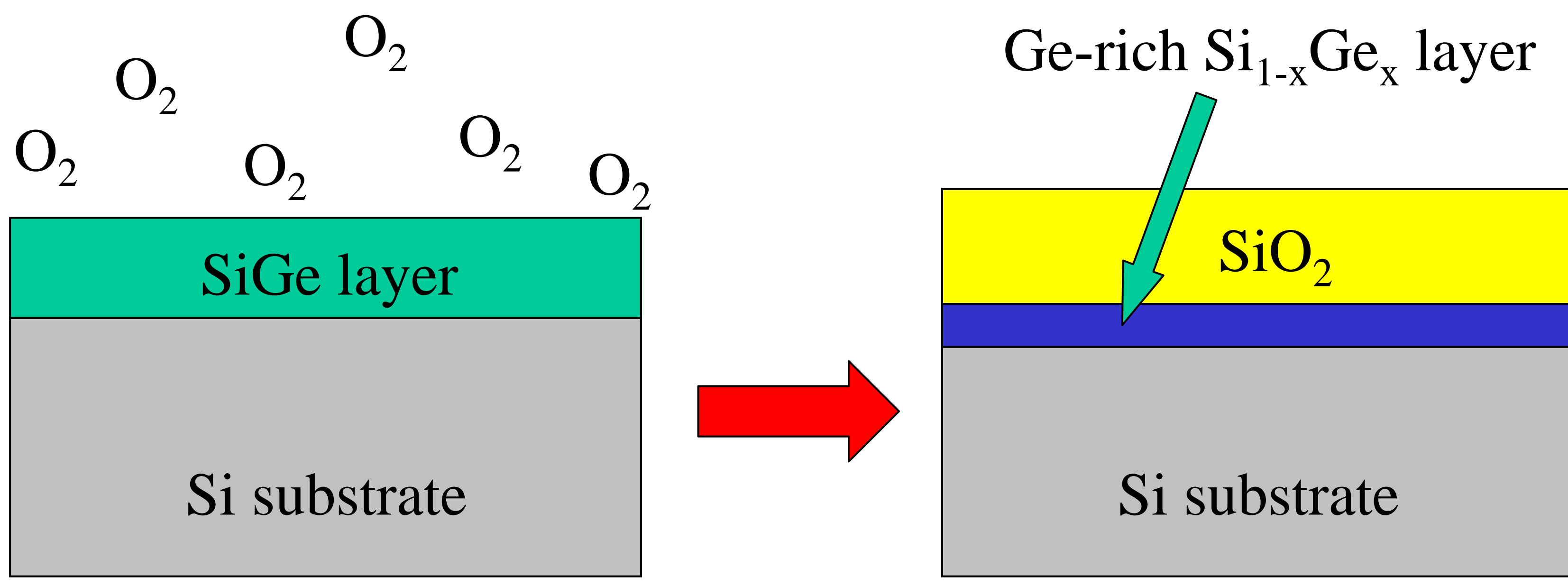
Write and erase operation of nanocrystal memory device



- To enable single-electron or few-electron memories by Coulomb blockade effect, smaller nanocrystals, ex. ~5 nm, are preferred.
- The Coulomb blockade effect of the nanocrystals makes the storage and operation of the memory device robust and fault-tolerant.

Experimental Results

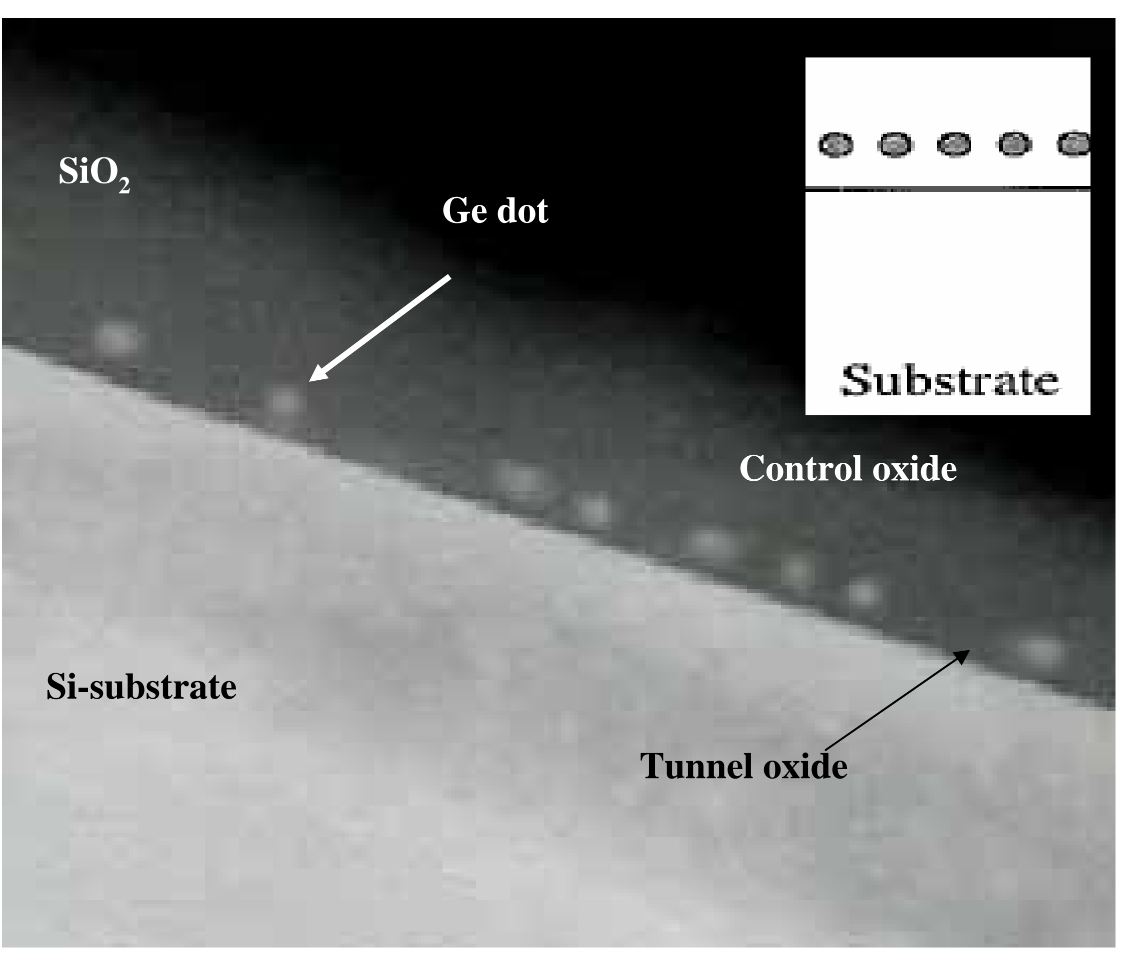
The segregation of Ge element from the oxidation process of SiGe

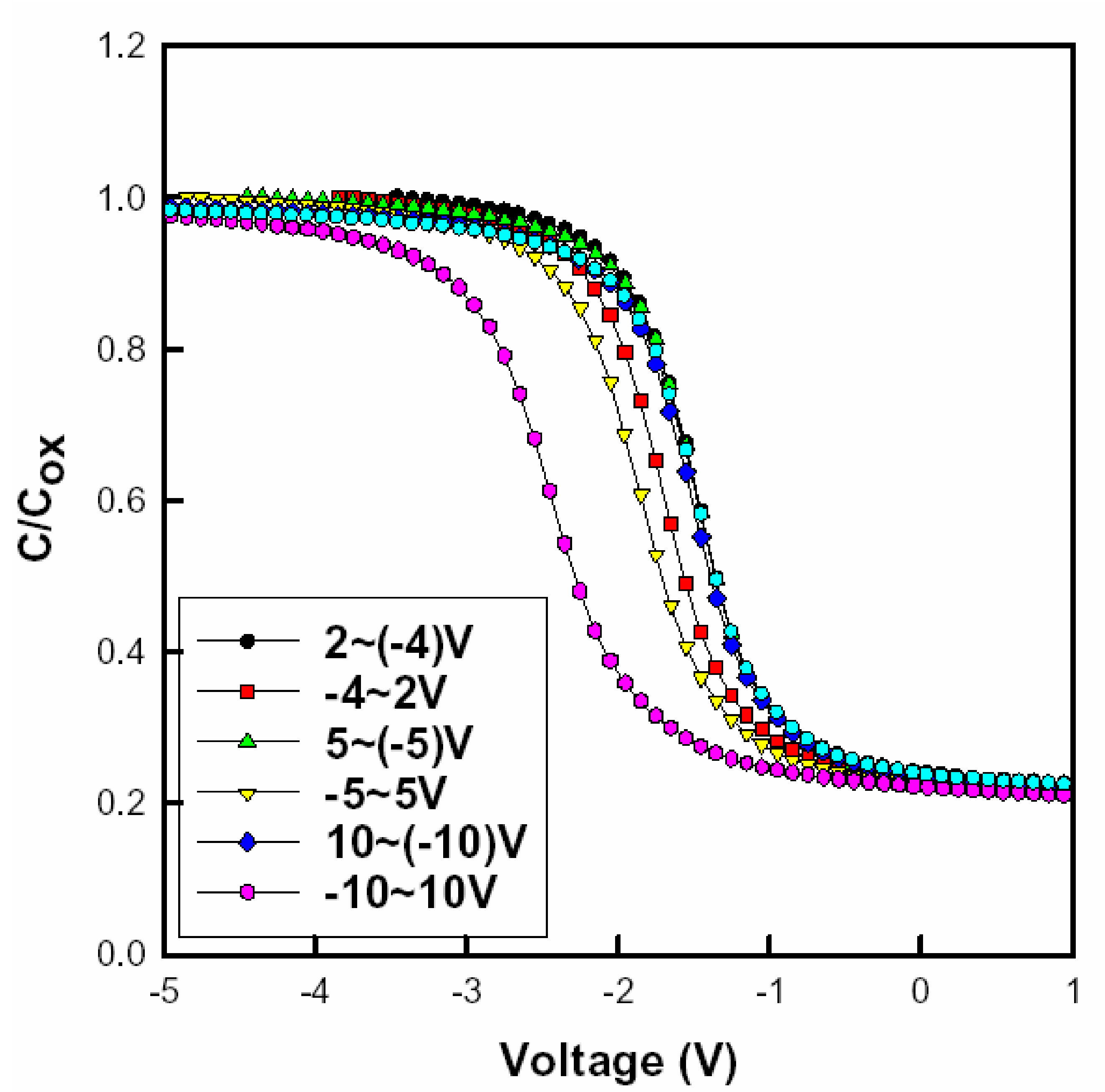


Process flow of fabricating Ge dots embedded in SiO_2

Standard clean, 4.5-nm tunnel oxide growth → LPCVD $Si_{1-x}Ge_x$ growth → Wet oxidation and Ge nanocrystals precipitate →

950°C N_2 RTA → Electrode patterned and sintered → Electrical measurement


SiO2
Ge dot
Substrate
Control oxide
Si-substrate
Tunnel oxide



5-V operation:

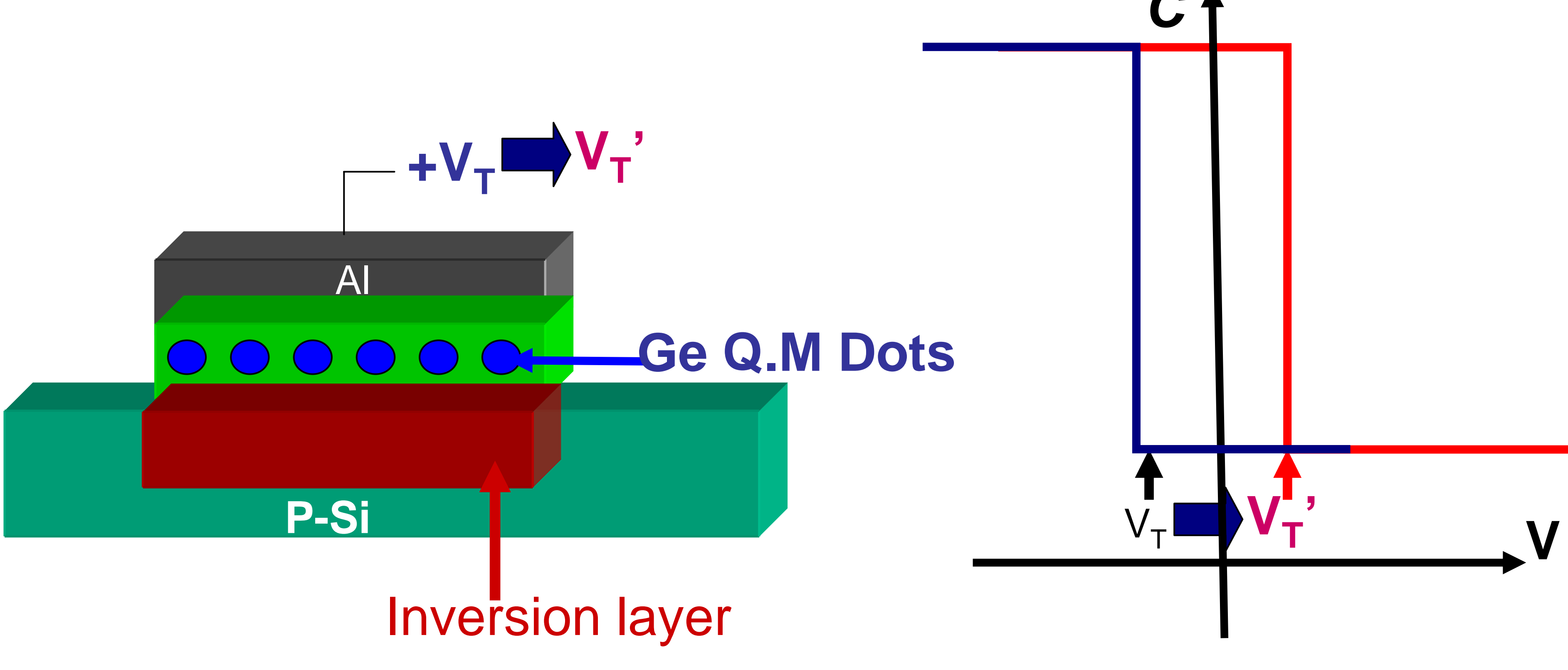
threshold voltage shift 0.42V

Threshold Voltage (V_T) Shift

功函數差　　　　空乏層電荷

$$V_T = |\Phi_{ms}| \; -Q_i/C_i \;\; |- Q_d/C_i| \; + \; 2\Phi_s$$

氧化層注入電荷　　　　強反轉定義之電壓



$$\Delta V_t = \frac{t_{control}}{\varepsilon_{ox}} \cdot Q_t$$

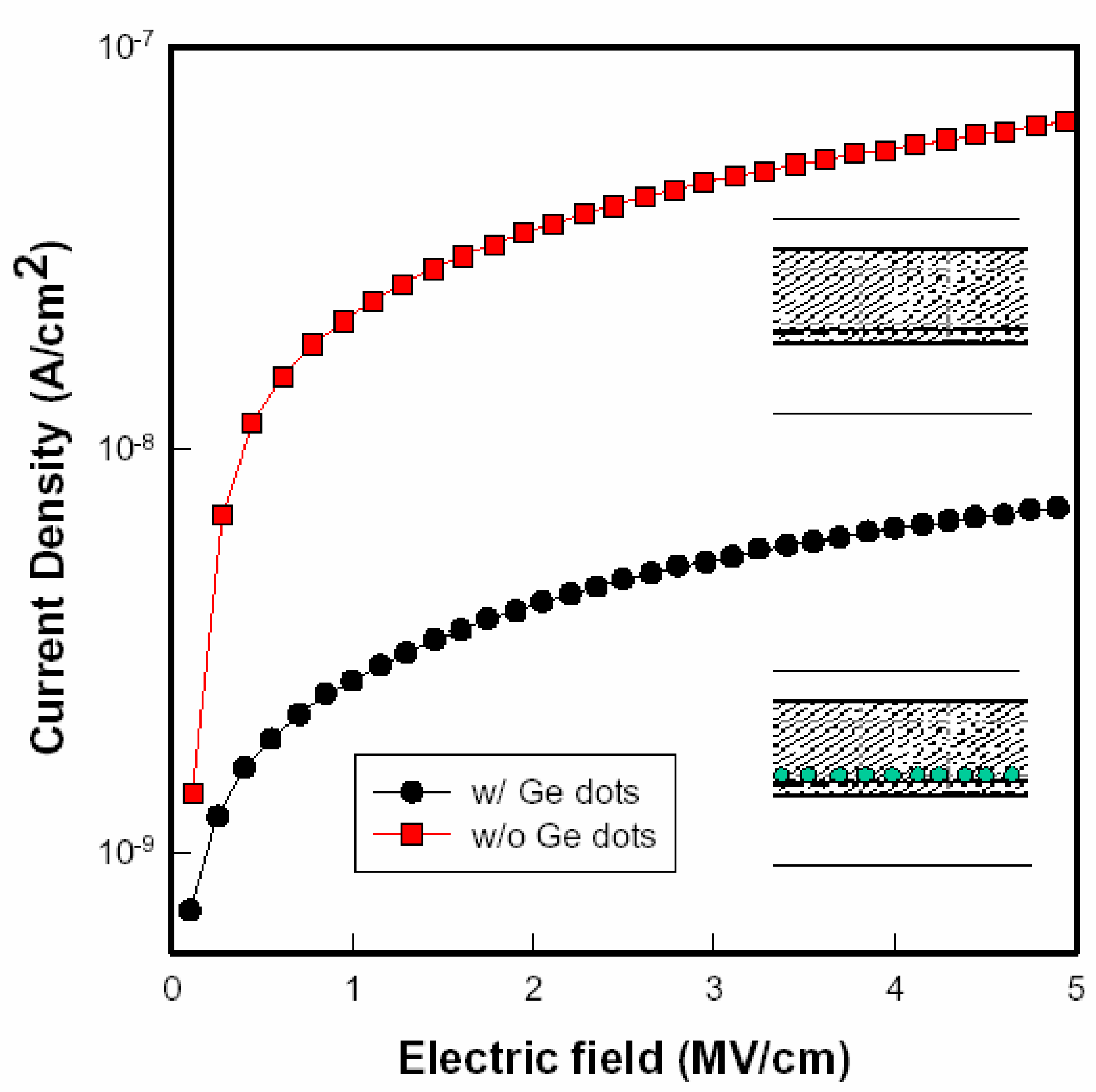
$$\Delta V_t = 1.14V$$

$$t_{control} \approx 40nm$$

$$\varepsilon_{ox} = 3.9 \times 8.85 \times 10^{-14} F / cm$$

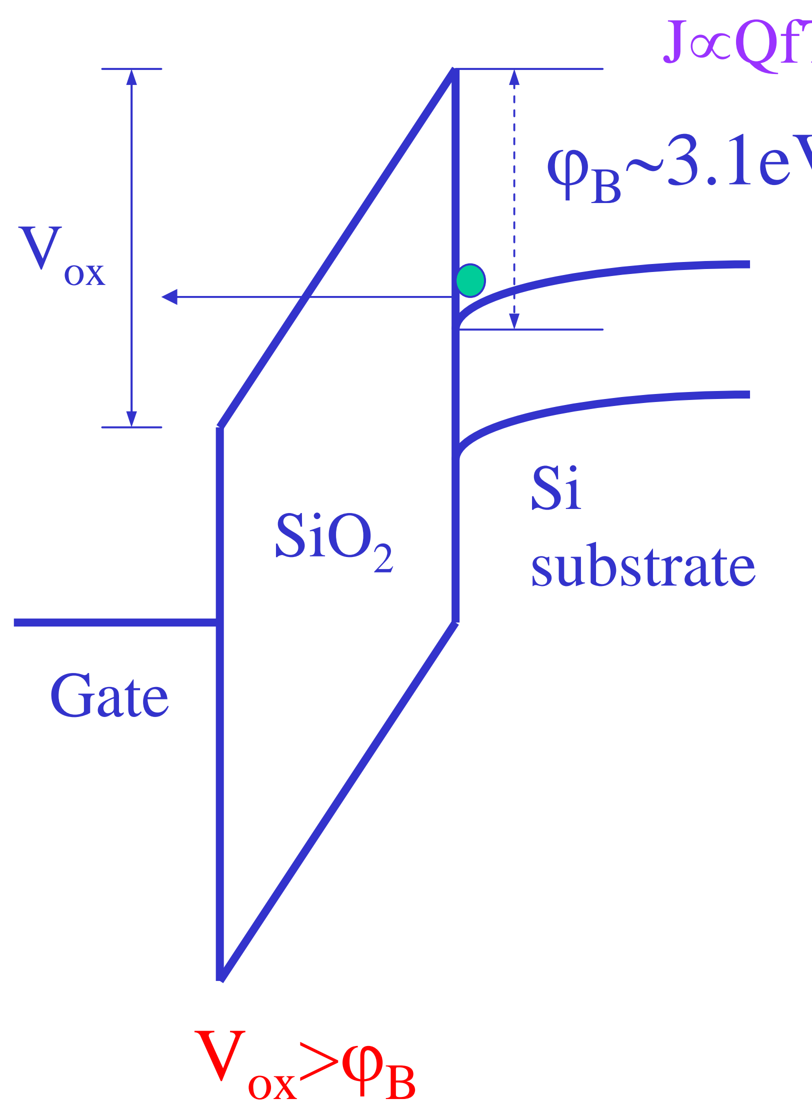
$$Q_t = 9.65 \times 10^{-8} C / cm^2$$

The C-V hysteresis was saturated at 10-V operation. The density of the Ge nanocrystal is electrically calculated to be around $6.2*10^{11}$ cm^{-2} .



Current Density (A/cm2)
10-7
10-8
10-9
0
1
2
3
4
5
Electric field (MV/cm)
w/ Ge dots
w/o Ge dots

Fowler-Nordheim Tunneling



J∝QfT

WKB approximation

$$J_{FN} = A\xi_{ox}^2 \exp\left[-\frac{B}{\xi_{ox}}\right]$$

$$barrier\ \ height : \varphi_B$$

$$Effective\ \ mass : 0.5m_e$$

$$A = \frac{q^3}{16\pi^2 \hbar \varphi_B}$$

$$B = \frac{4}{3}\frac{(2m_{ox})^{1/2}}{q\hbar}\varphi_B^{3/2}$$

Fowler-Nordheim tunneling

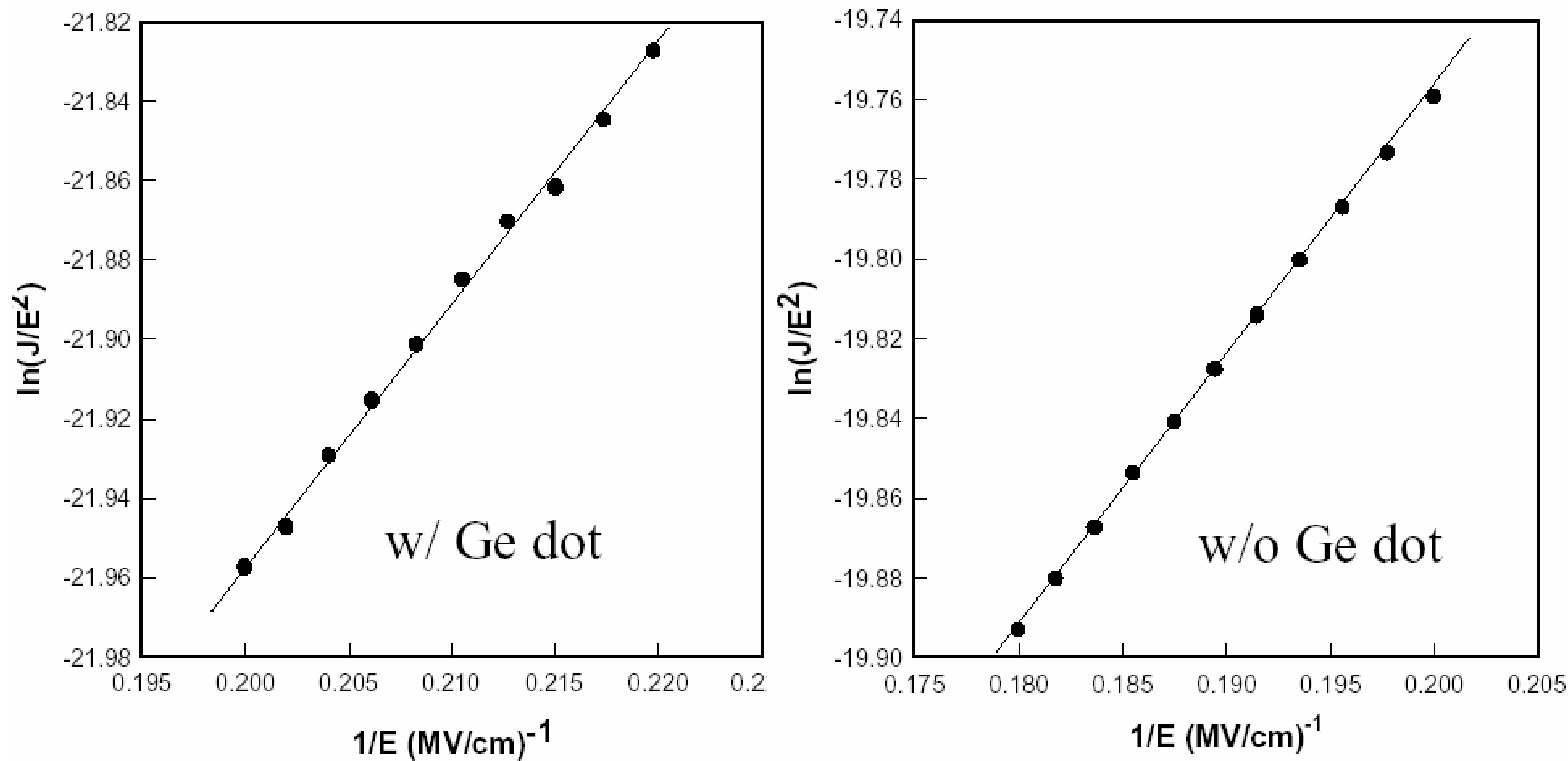
$$J = \alpha E^2 \exp\left[\frac{-E_c}{E}\right]$$

$$\alpha = \frac{q^3}{8\pi h \phi_b} \frac{m}{m^*}$$

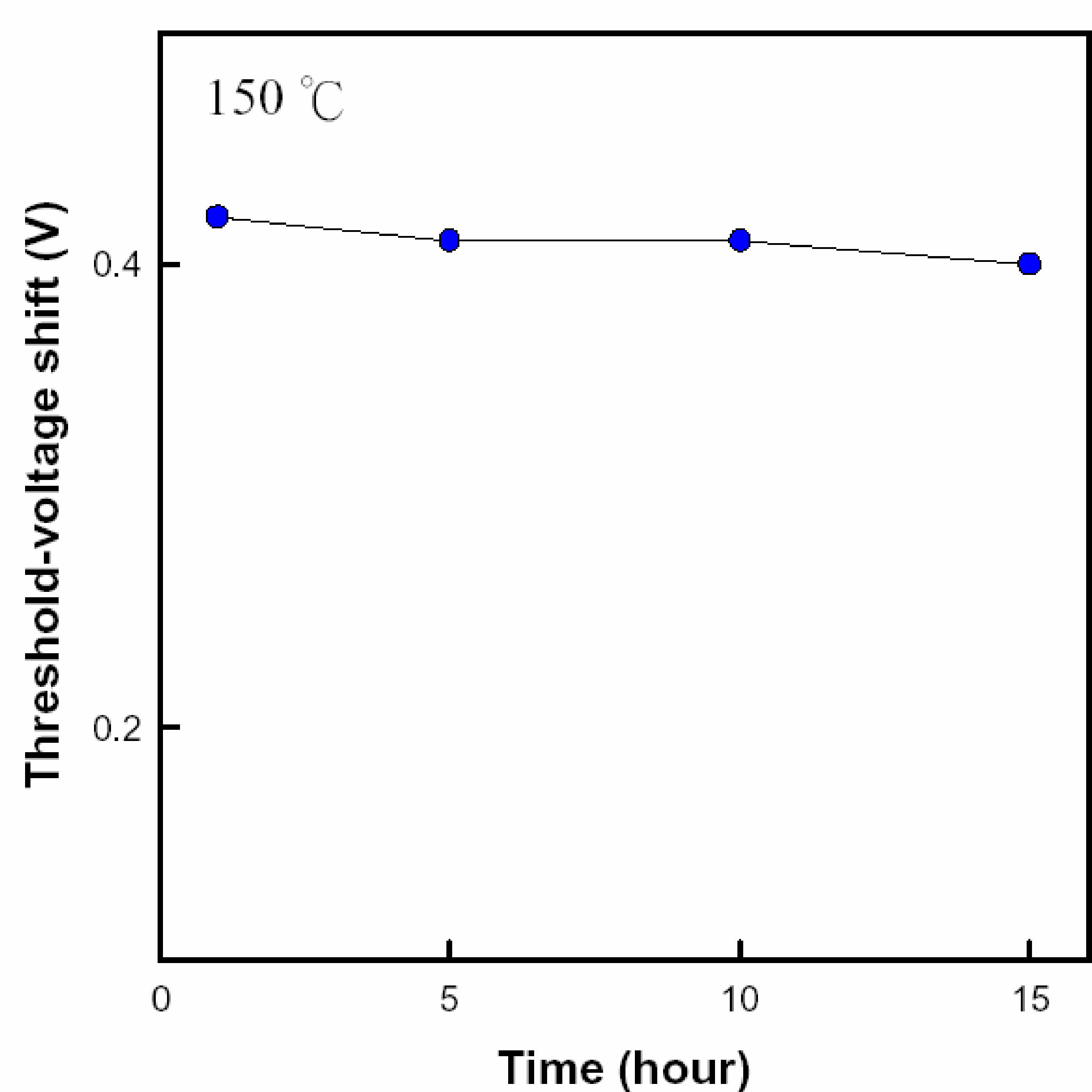
M^*= the effective mass of an electron in the band gap of SiO_2. (0.42m)

$$E_c = 4\sqrt{2m^*} \frac{\phi_b^{3/2}}{3\hbar q}$$

$$\log\left(\frac{J}{E^2}\right) \propto (1/E)$$



-21.82
-21.84
-21.86
-21.88
-21.90
-21.92
-21.94
-21.96
-21.98
$ln(J/E^2)$
0.195
0.200
0.205
0.210
0.215
0.220
1/E $(MV/cm)^{-1}$
w/ Ge dot
-19.74
-19.76
-19.78
-19.80
-19.82
-19.84
-19.86
-19.88
-19.90
$ln(J/E^2)$
0.175
0.180
0.185
0.190
0.195
0.200
0.205
1/E $(MV/cm)^{-1}$
w/o Ge dot

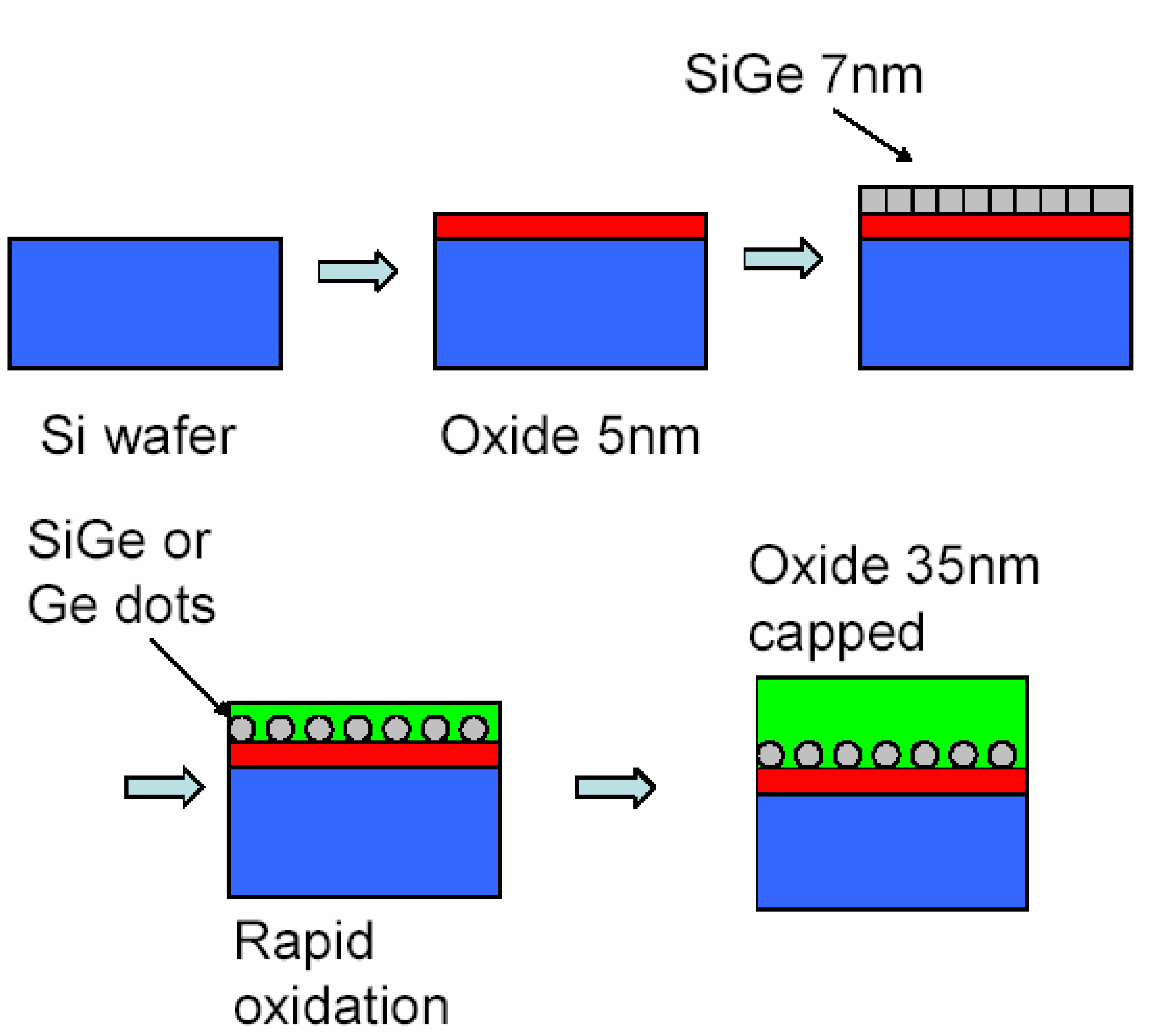


150 ℃
Threshold-voltage shift (V)
0.4
0.2
0
5
10
15
Time (hour)

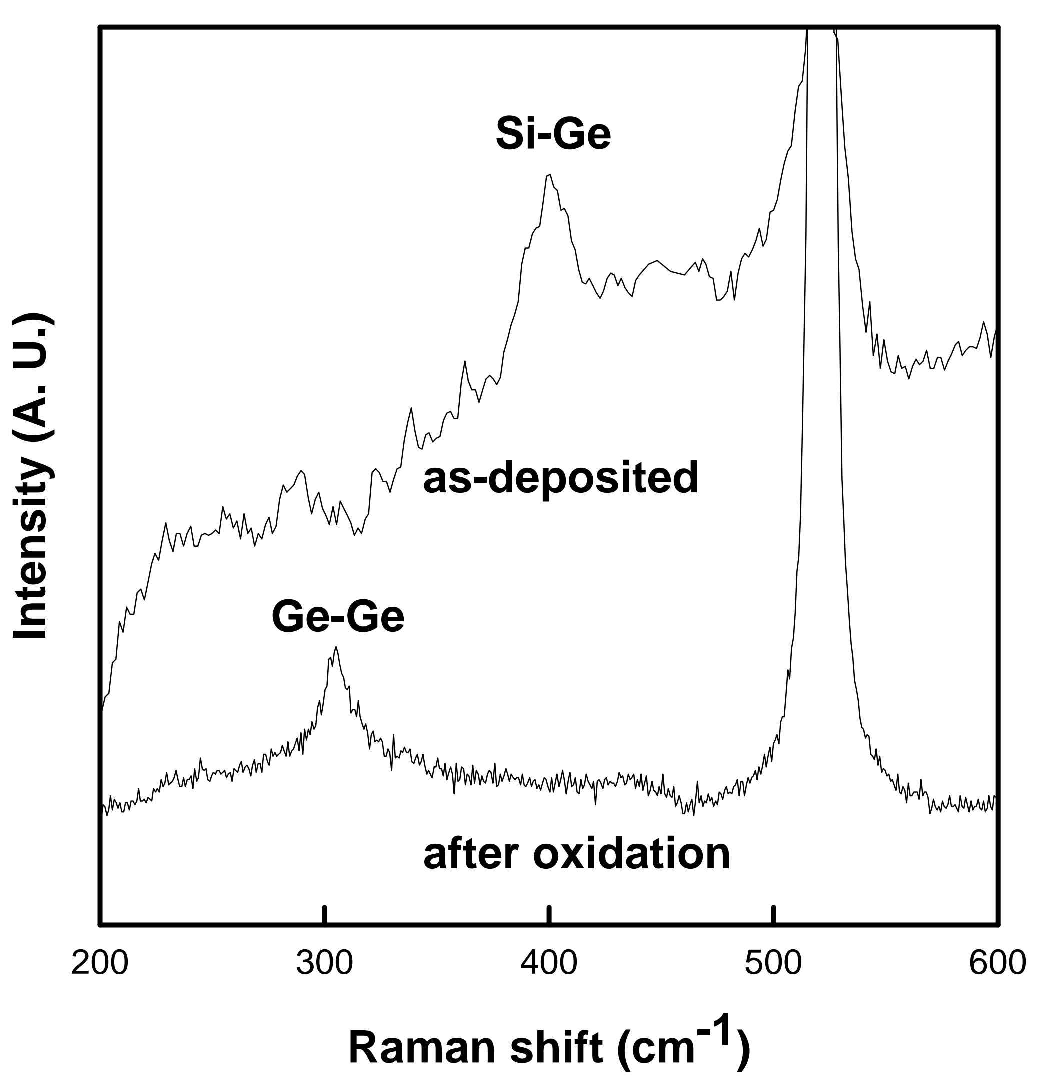
Summary (1)

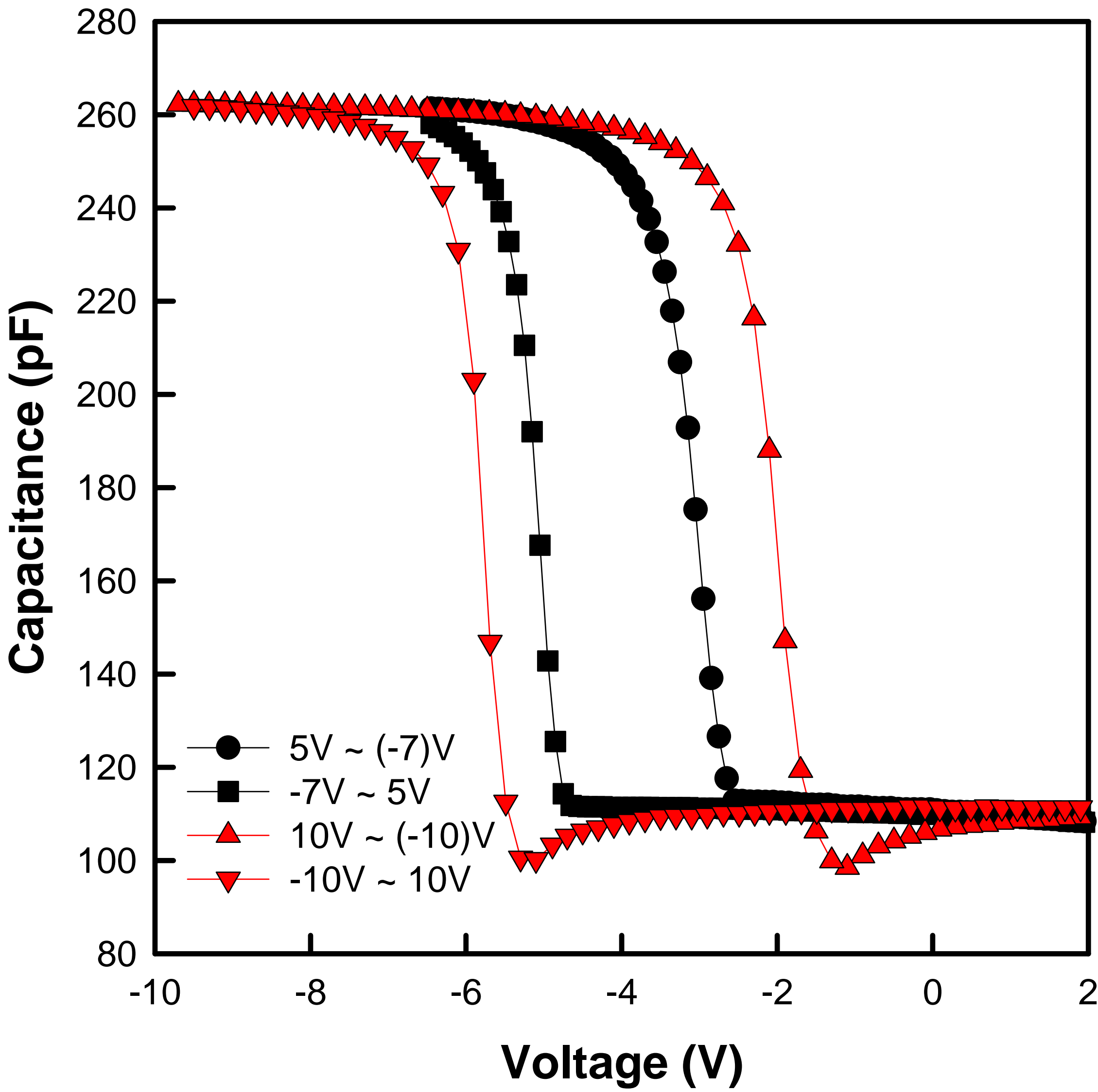
- Ge nanocrystal memory device with 4.5-nm tunnel oxide is demonstrated.
- A low operating voltage, 5V, is implemented and a significant threshold voltage shift (0.42V) is observed.
- The density of the Ge nanocrystals is about $6.2*10^{11}$ cm^{-2}.
- The retention characteristics are tested to be robust.

Rapid oxidation of thin SiGe film down to 10 nm


SiGe 7nm
Si wafer
Oxide 5nm
SiGe or
Ge dots
Oxide 35nm
capped
Rapid
oxidation

Raman spectroscopy of the gate stack





Capacitance (pF)
280
260
240
220
200
180
160
140
120
100
80
-10
-8
-6
-4
-2
0
2
Voltage (V)
5V ~ (-7)V
-7V ~ 5V
10V ~ (-10)V
-10V ~ 10V

Summary (2)

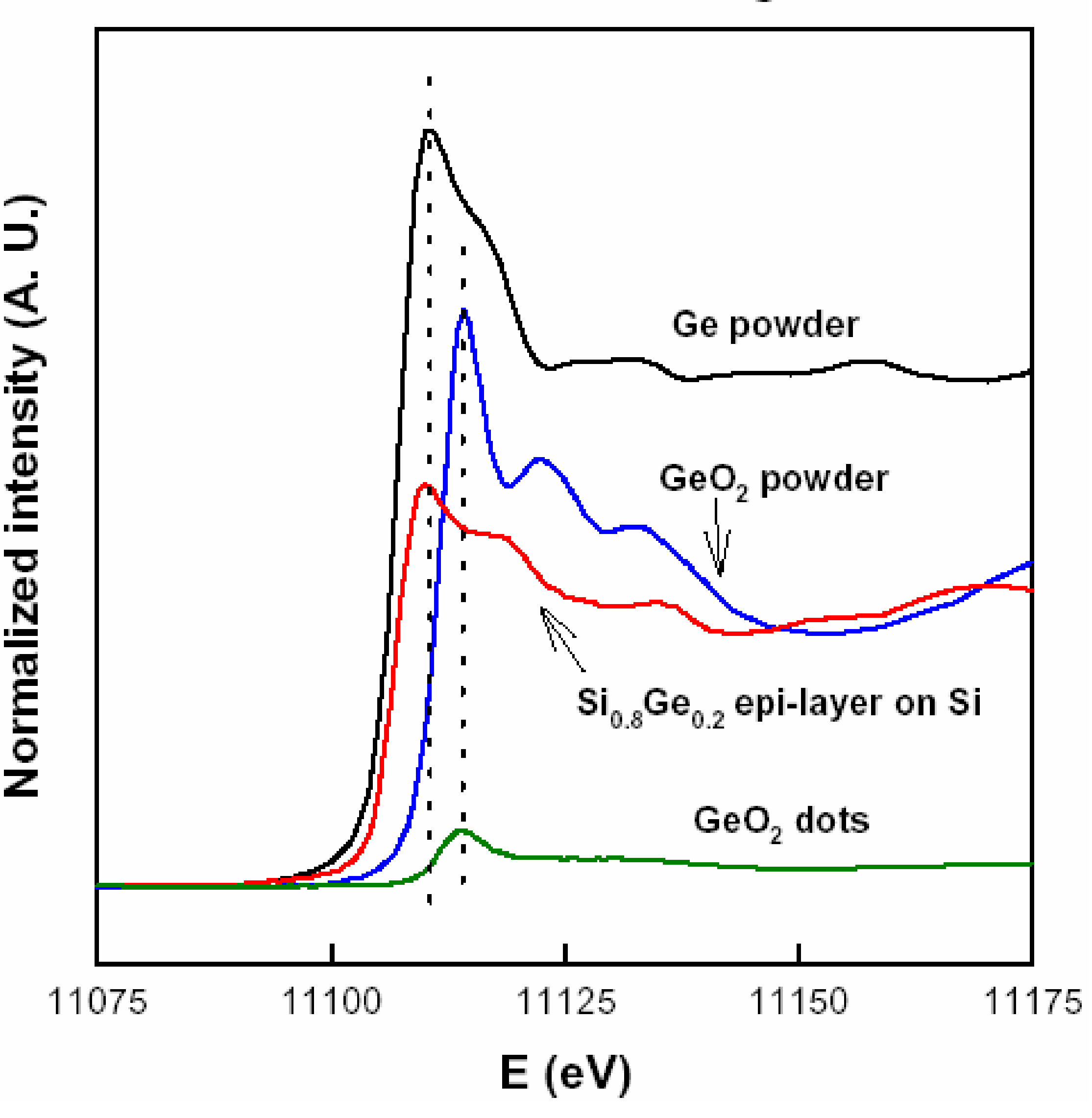
- Ge precipitation of the rapid oxidation of SiGe is observed in Raman spectroscopy.
- Via the suitable control of the rapid oxidation process, SiGe or Ge dots can be realized as expected.

A distributed charge storage of GeO_2 nano-dots (over oxidation of Ge nano-dots)

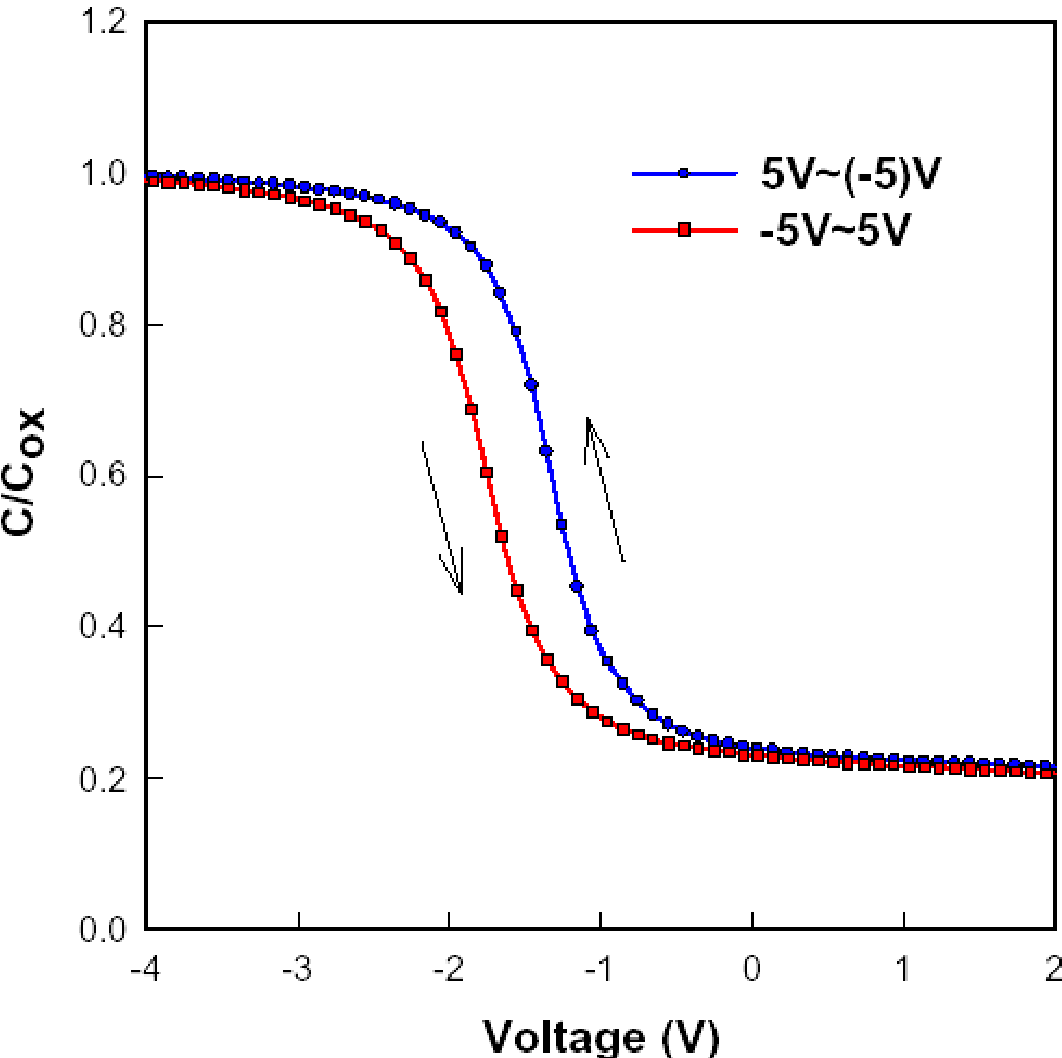
X-ray Absorption Near Edge Structure (XANES)

- In X-ray absorption near edge structure (XANES), a core electron is excited to higher bound or quasi-bound states, which contain information about coordination geometry and electronic aspects of the absorbing atom.

- Among most of the XANES study, the standard materials with known valence is utilized as references, and compared with unknown samples.
- The measurements are frequently qualitatively analyzed, not quantitatively.
- Nowadays, almost all experiments of X-ray absorption spectroscopy are using synchronizing radiation as light source.
- X-ray source: National Synchrotron Radiation Research Center.

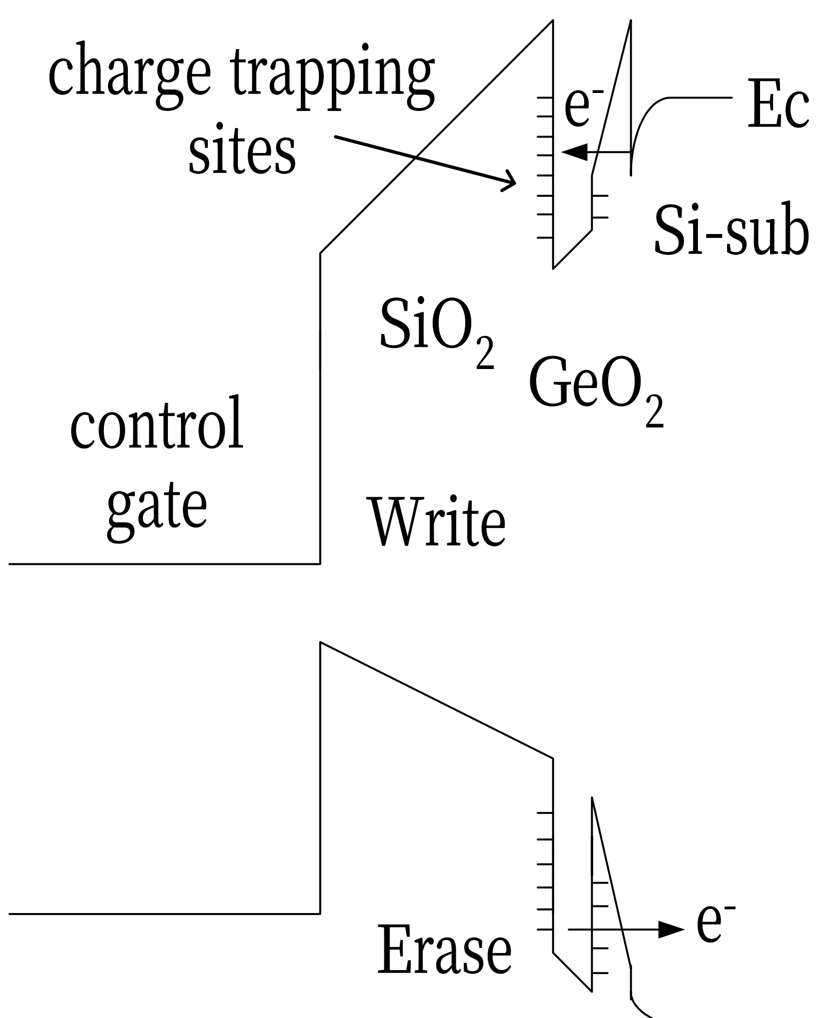


XANES at Ge K-edge
Normalized intensity (A. U.)
Ge powder
GeO2 powder
Si0.8Ge0.2 epi-layer on Si
GeO2 dots
11075
11100
11125
11150
11175
E (eV)



5V~(-5)V
-5V~5V
C/Cox
Voltage (V)
1.2
1.0
0.8
0.6
0.4
0.2
0.0
-4
-3
-2
-1
0
1
2

The charge storage mechanism of GeO_2 nanodots embedded in SiO_2



Summary (3)

- XANES is a useful analysis tool for the microscopic structures of the nano-dots.
- Obvious charge trapping effects are observed in the GeO_2 nano-dots embedded in SiO_2.
- It is deduced that the insulating GeO_2 can be utilized as a storage element acting as silicon nitride.

Semiconductor memory with tungsten (W) nanodot

The major advantages of metal nanodots over their semiconductor counterparts:

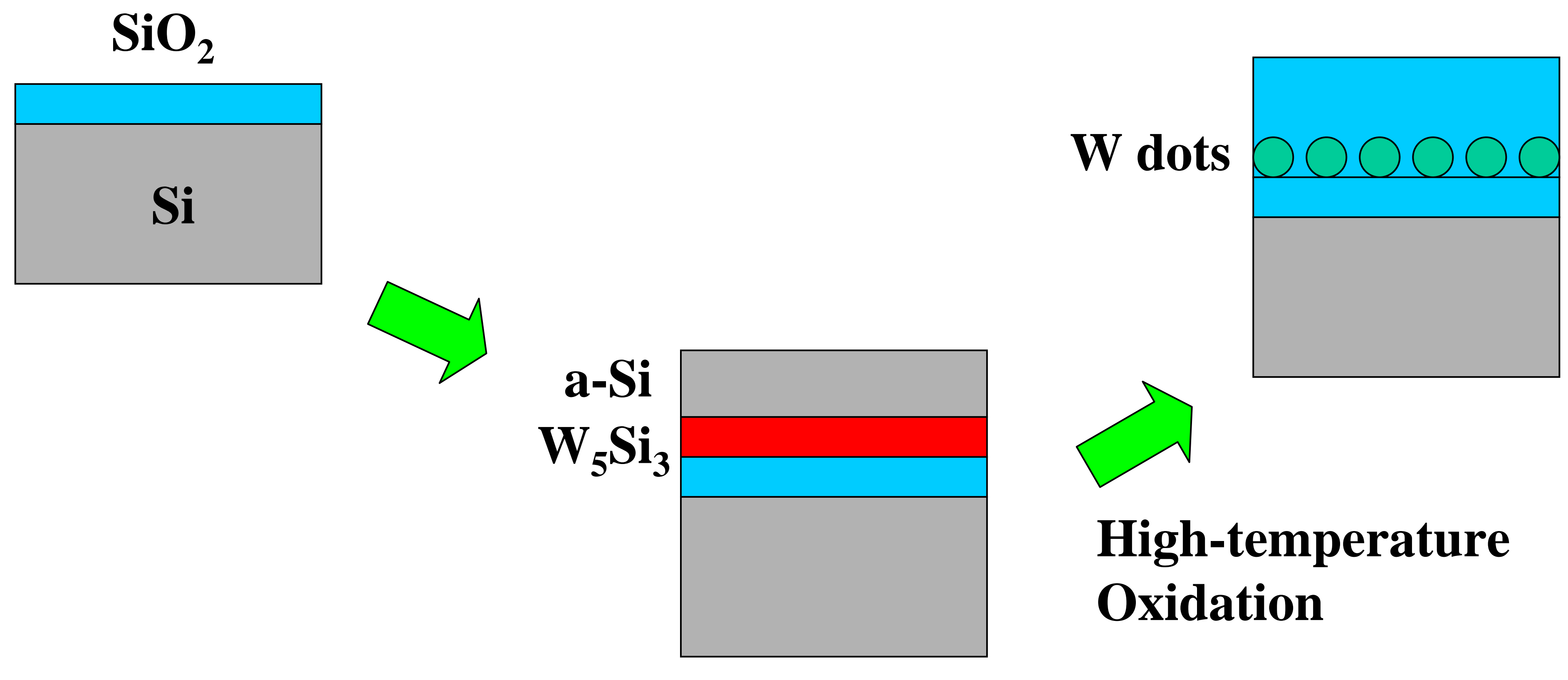
(1) stronger coupling with the conduction channel

(2) a wide range of available work functions

- To enable single-electron or few-electron memories by Coulomb blockade effect, smaller nanocrystals are preferred.
- However, for semiconductor nanocrystals, the band gap of the nanocrystals is widened in comparison with that of the bulk materials due to the multi-dimensional carrier confinement, which compromises the retention time.

- The work function of metal thin films does not deviate from their bulk value dramatically down to about **0.4 nm** in thickness.
- We can exploit the Coulomb blockade effect better with metal nanocrystals to achieve ultra low-power memories without compromising the retention time from quantum mechanical confinement effects.

Process Flow of Fabricating W Nanodots



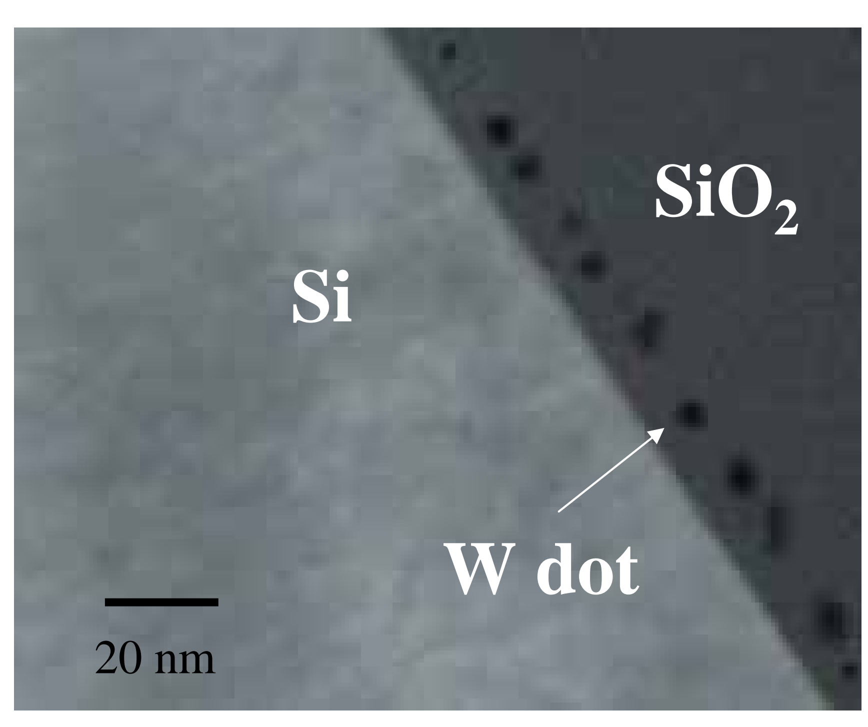
Parameters of the process

- Dry oxide 4.5 nm, 925 ℃, APCVD.
- W silicide 8 nm, a-Si 10 nm, sputtering.
- Oxidation of the gate stack, 900 ℃.

The nature of the oxidation of tungsten silicide

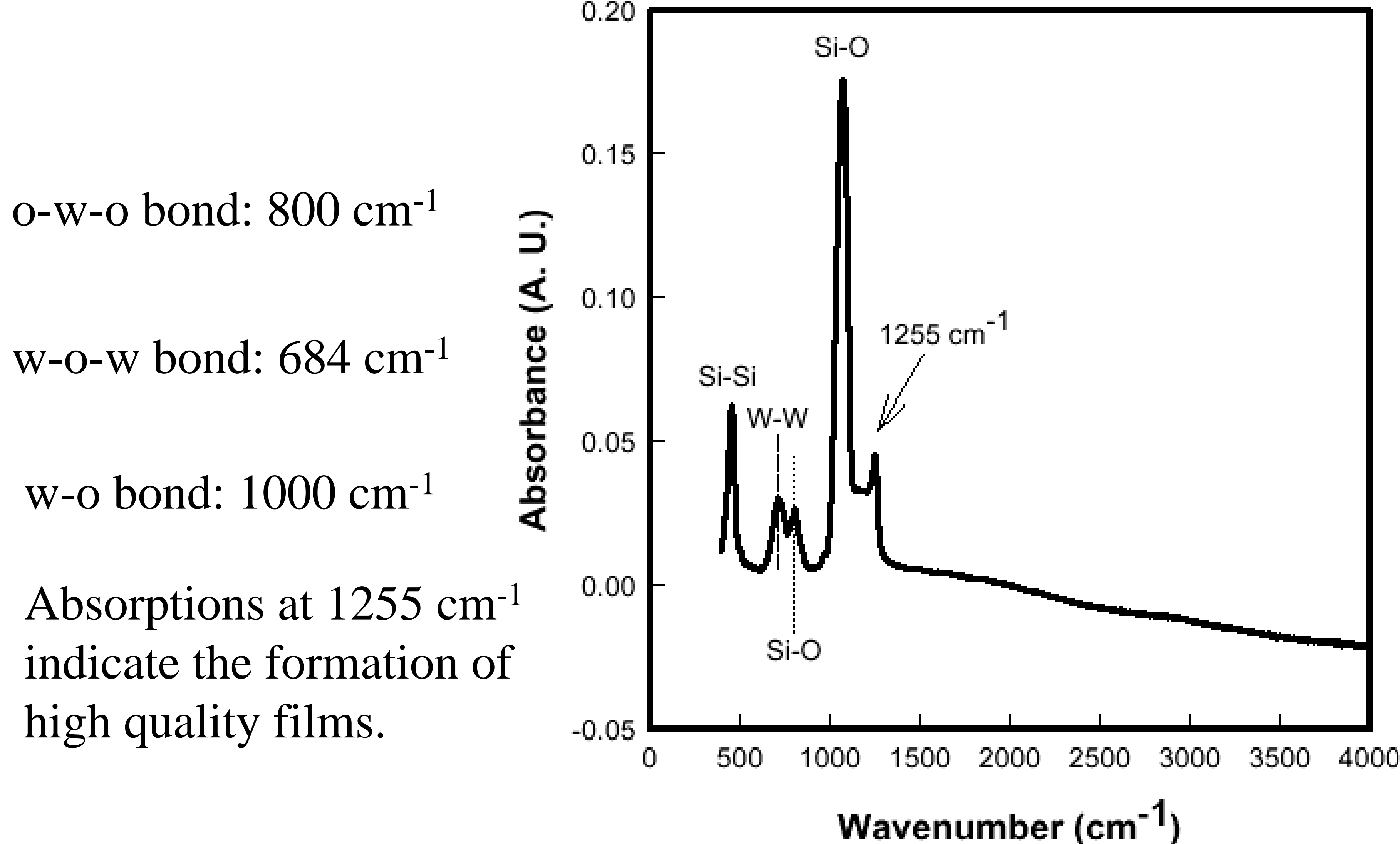
- For tungsten silicide films deposited on SiO_2, in the initial stage of the oxidation, the removal of Si from the silicide layer leads directly to the formation of free W.

TEM micrograph of the W dots



- The mean size and aerial density of the W nanocrystals are found to be 4.5 nm and $3.7 \times 10^{11}/cm^2$, respectively.

FTIR spectrum of the sample after high-temperature oxidation



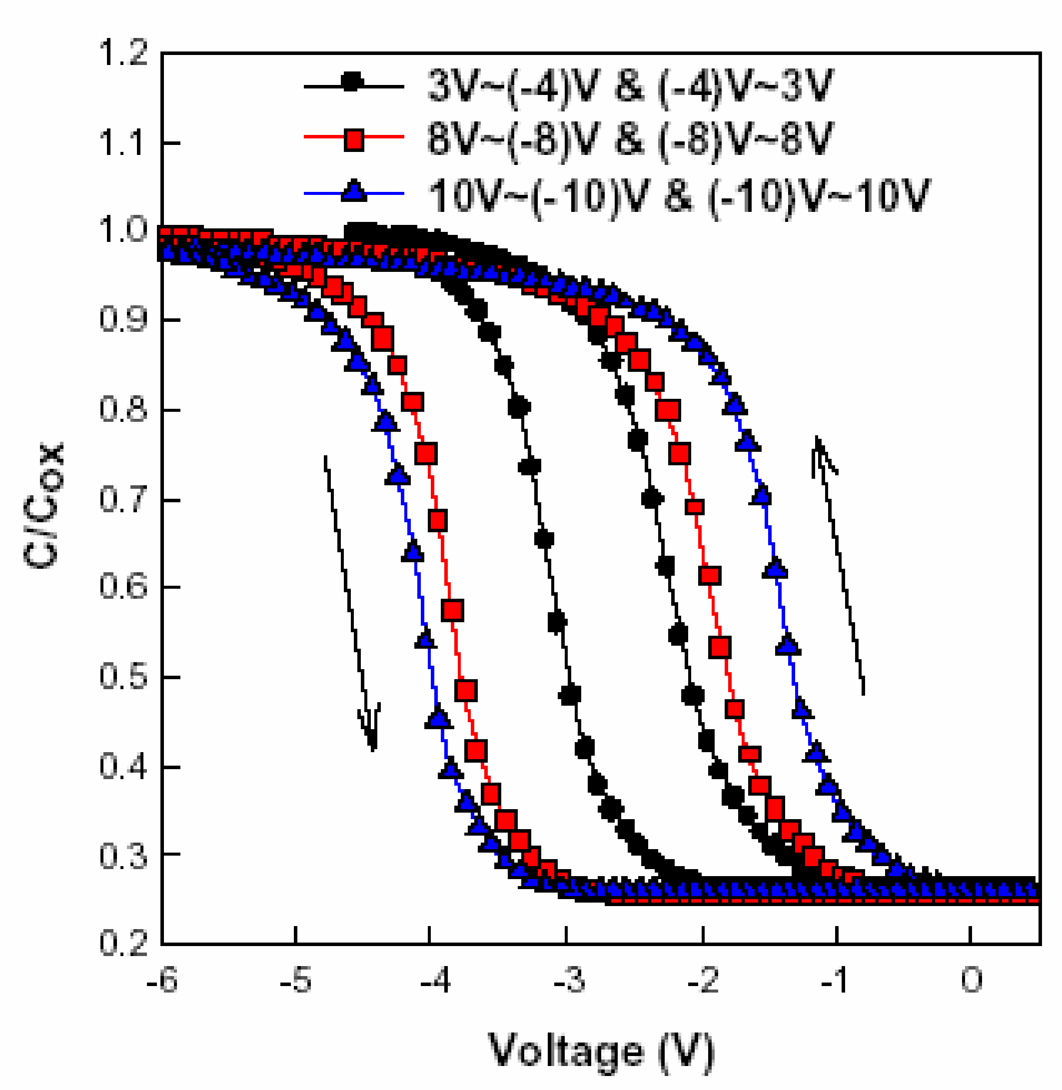
o-w-o bond: 800 cm^{-1}

w-o-w bond: 684 cm^{-1}

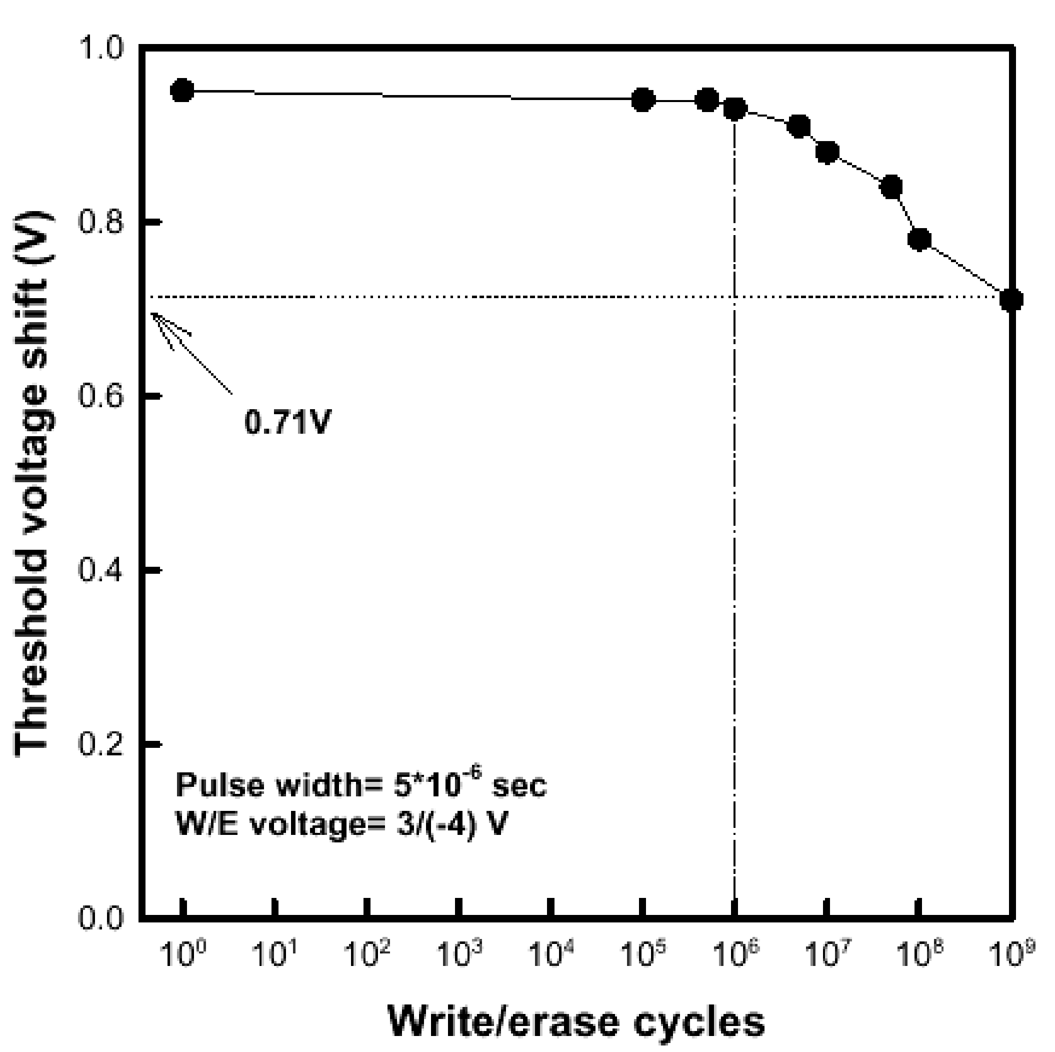
w-o bond: 1000 cm^{-1}

Absorptions at 1255 cm^{-1} indicate the formation of high quality films.

Electron charging and discharging effects of tungsten (W) nanocrystals



The endurance characteristics of the W nanocrystal memory device

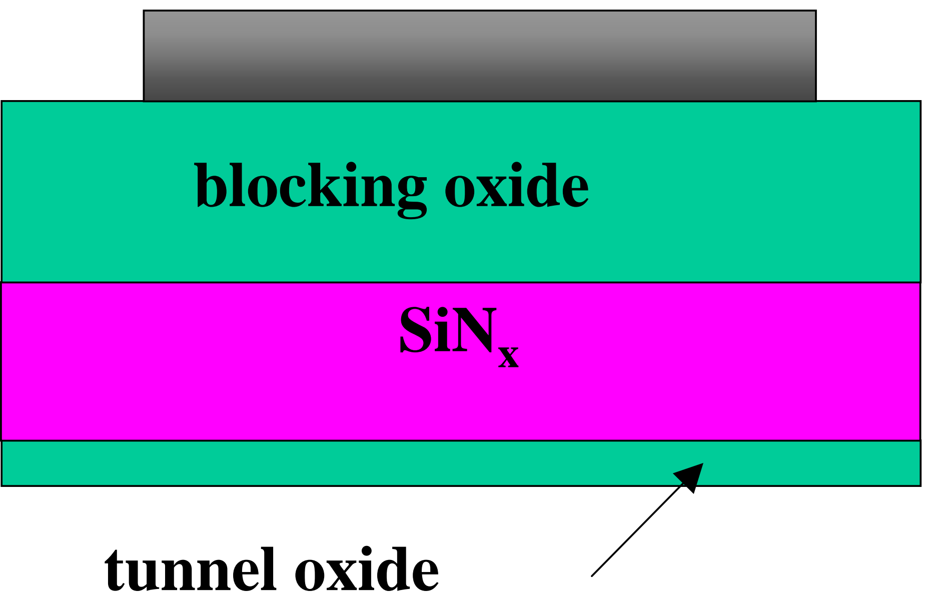


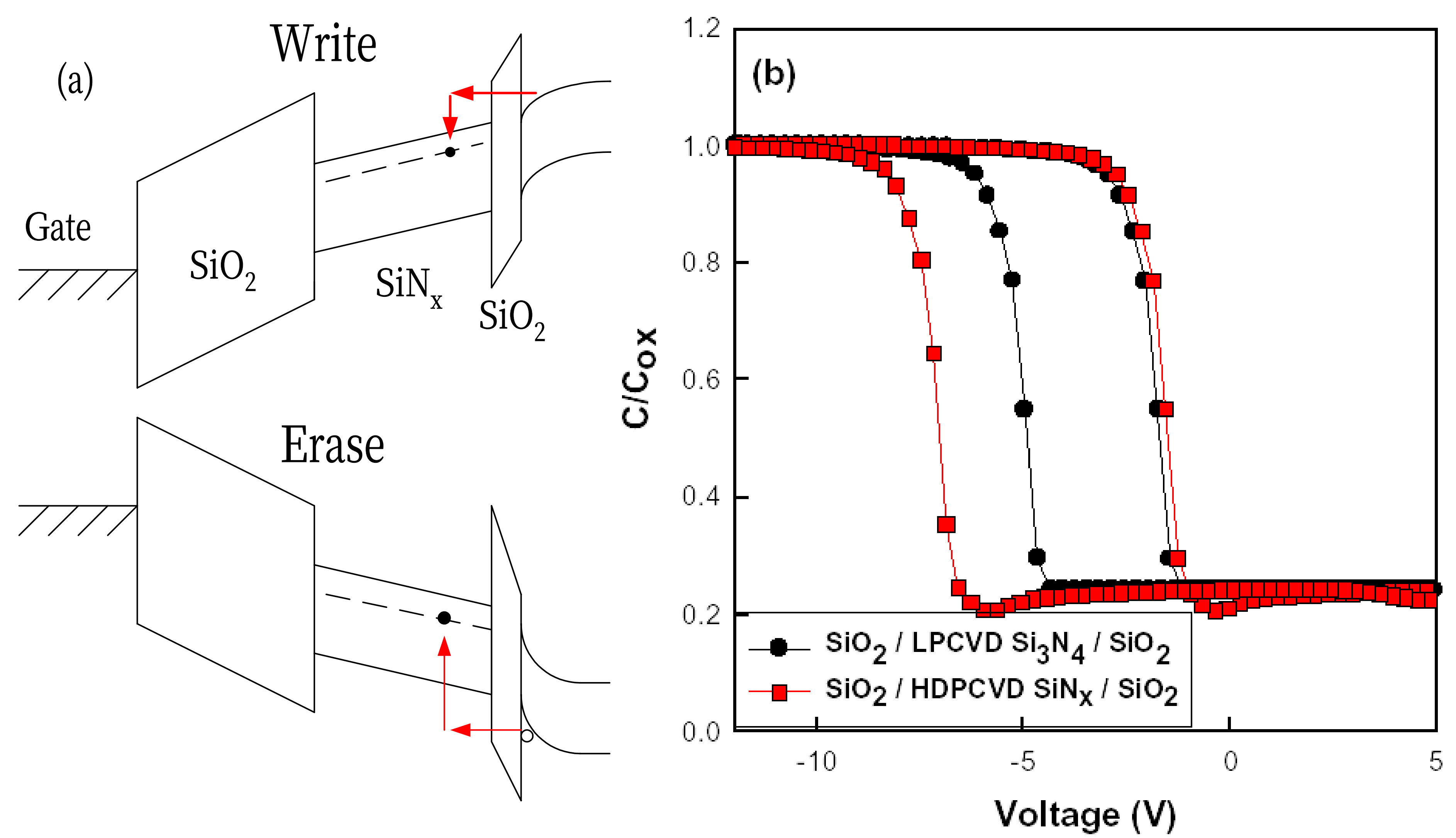
Summary (4)

- W nano-dots are fabricated based on the oxidation of tungsten silicide and the mean size and aerial density of the W nanocrystals are estimated to be 4.5 nm and $3.7\times10^{11}/cm^2$, respectively.
- Threshold voltage shift of 0.95 V under 3-V operation was observed by C-V hysteresis, which is, to our knowledge, the largest memory window in the study of low-power nanocrystal memory device.
- The endurance behavior of W nano-dots memory device is tested to be robust up to 10^6 cycles.

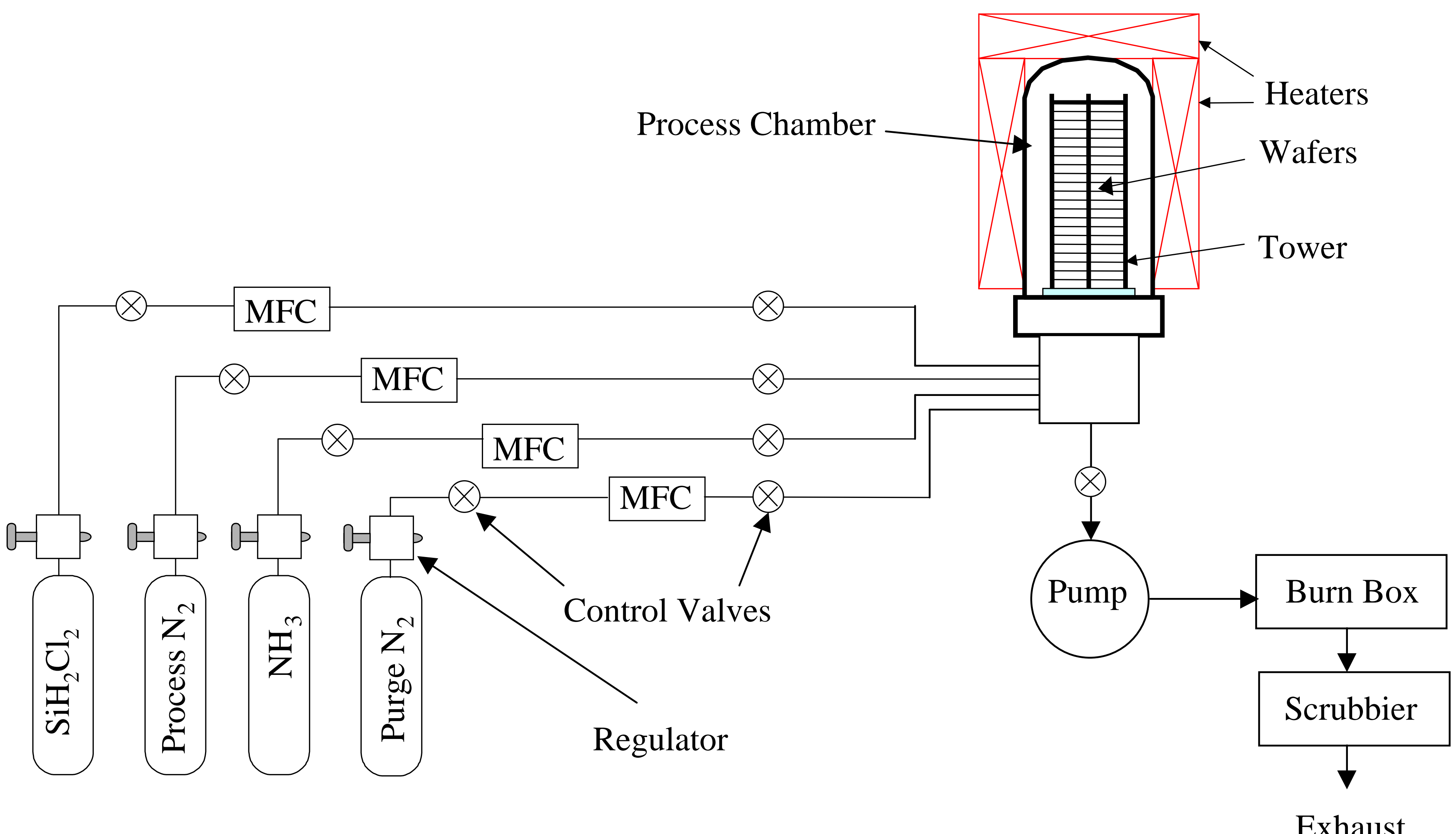
The study on SONOS nonvolatile memory technology

ONO gate stack for SONOS technology

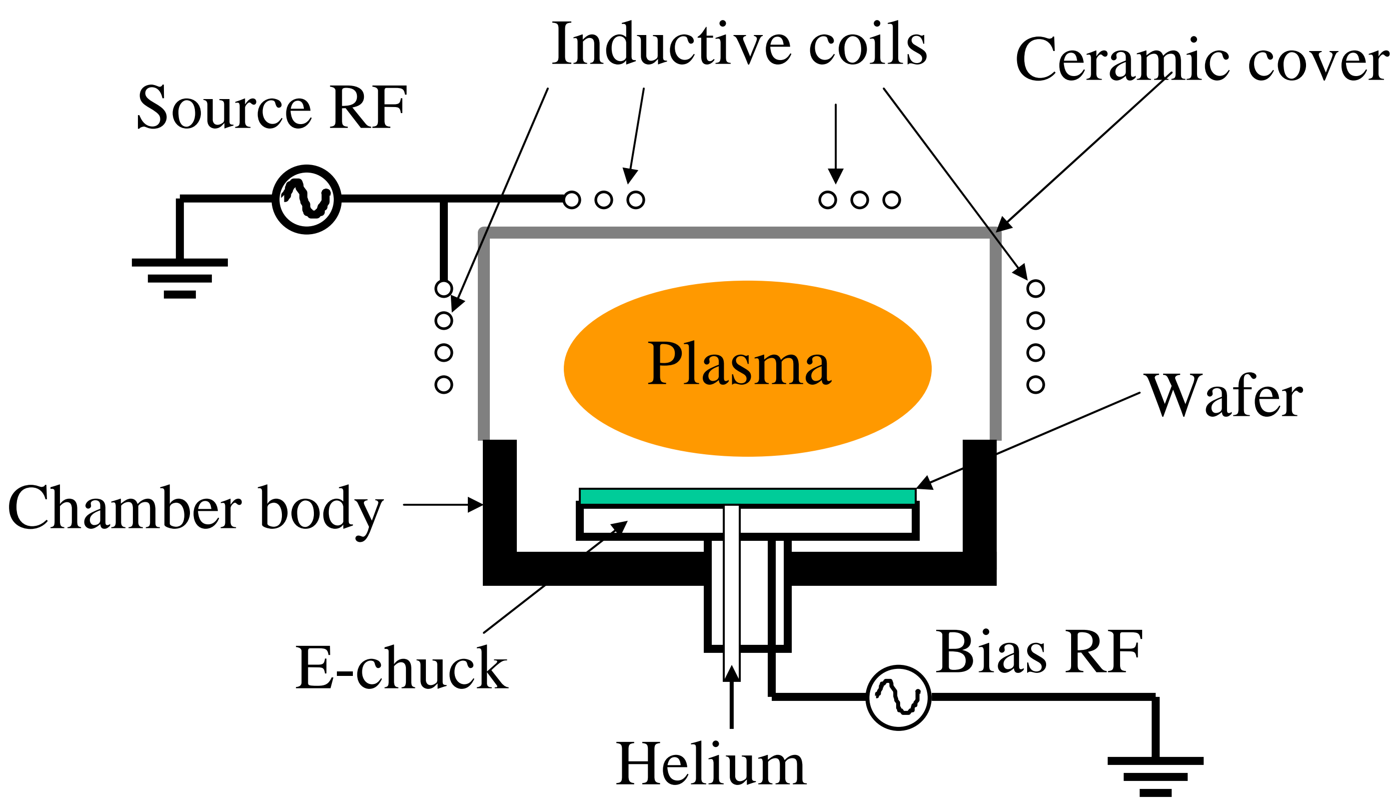


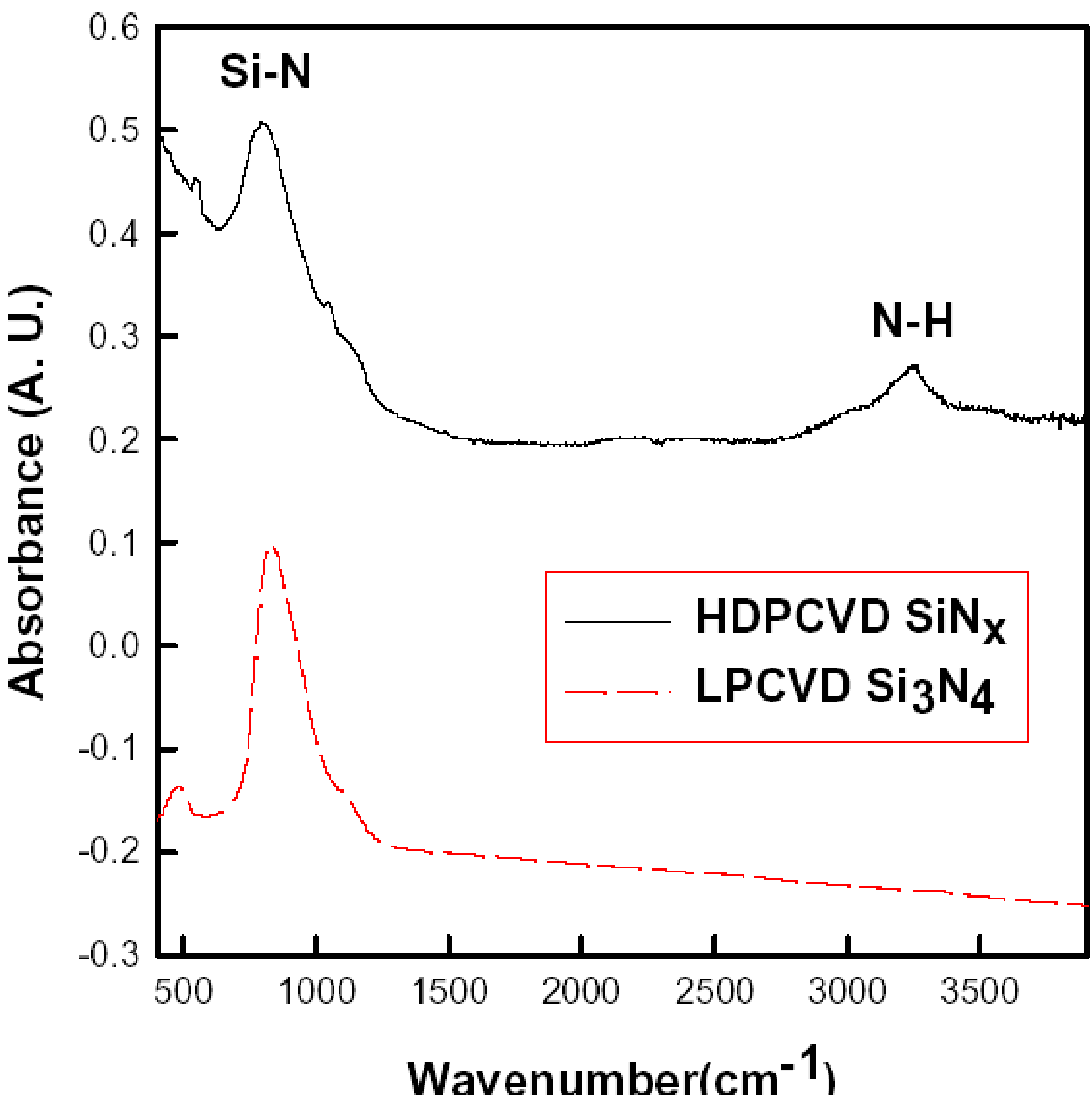

(a)
Write
Gate
SiO2
SiNx
SiO2
Erase
(b)
1.2
1.0
0.8
0.6
0.4
0.2
0.0
C/Cox
-10
-5
0
5
Voltage (V)
SiO2 / LPCVD Si3N4 / SiO2
SiO2 / HDPCVD SiNx / SiO2

Silicon Nitride LPCVD System

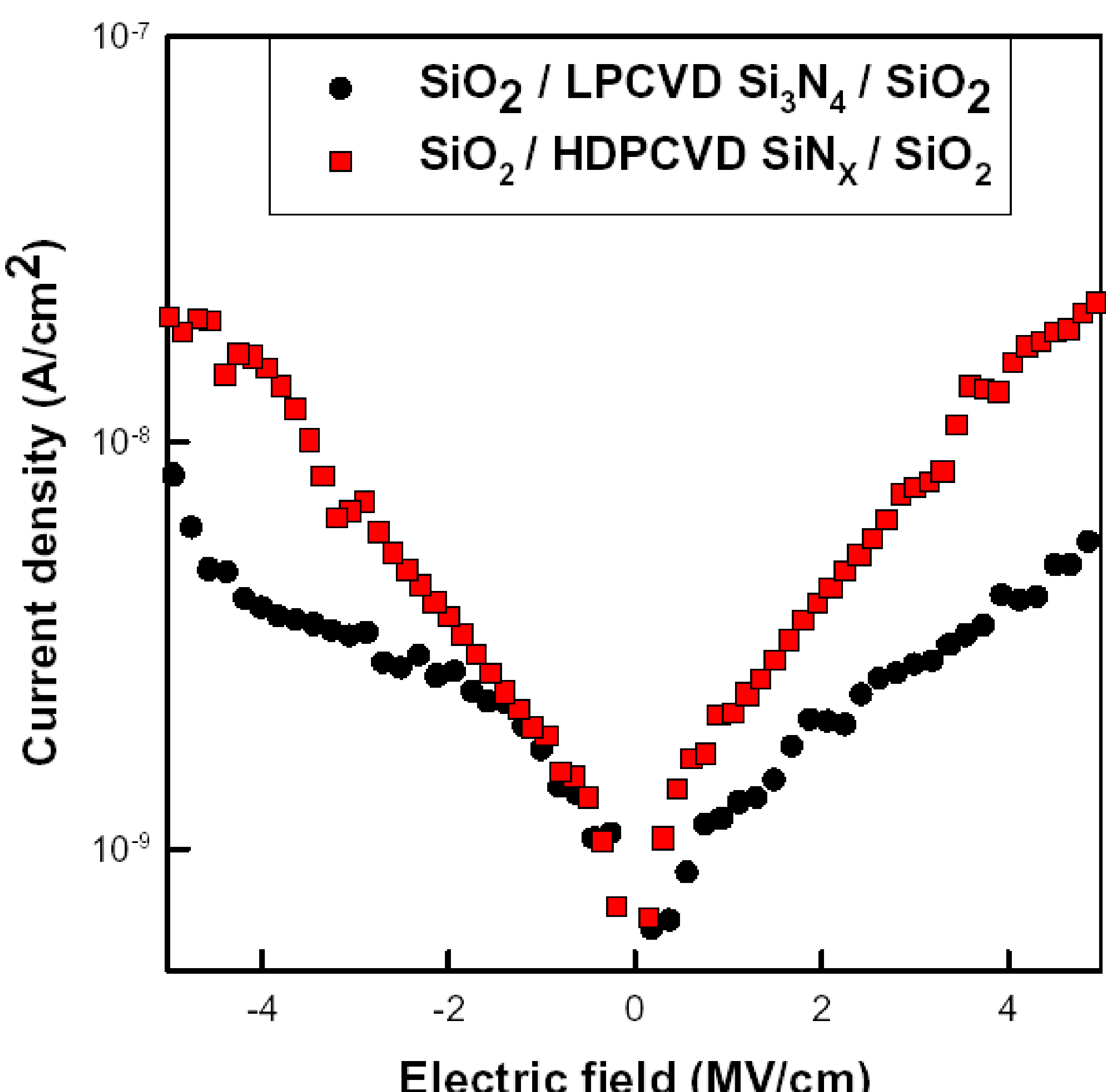


High Density Plasma CVD

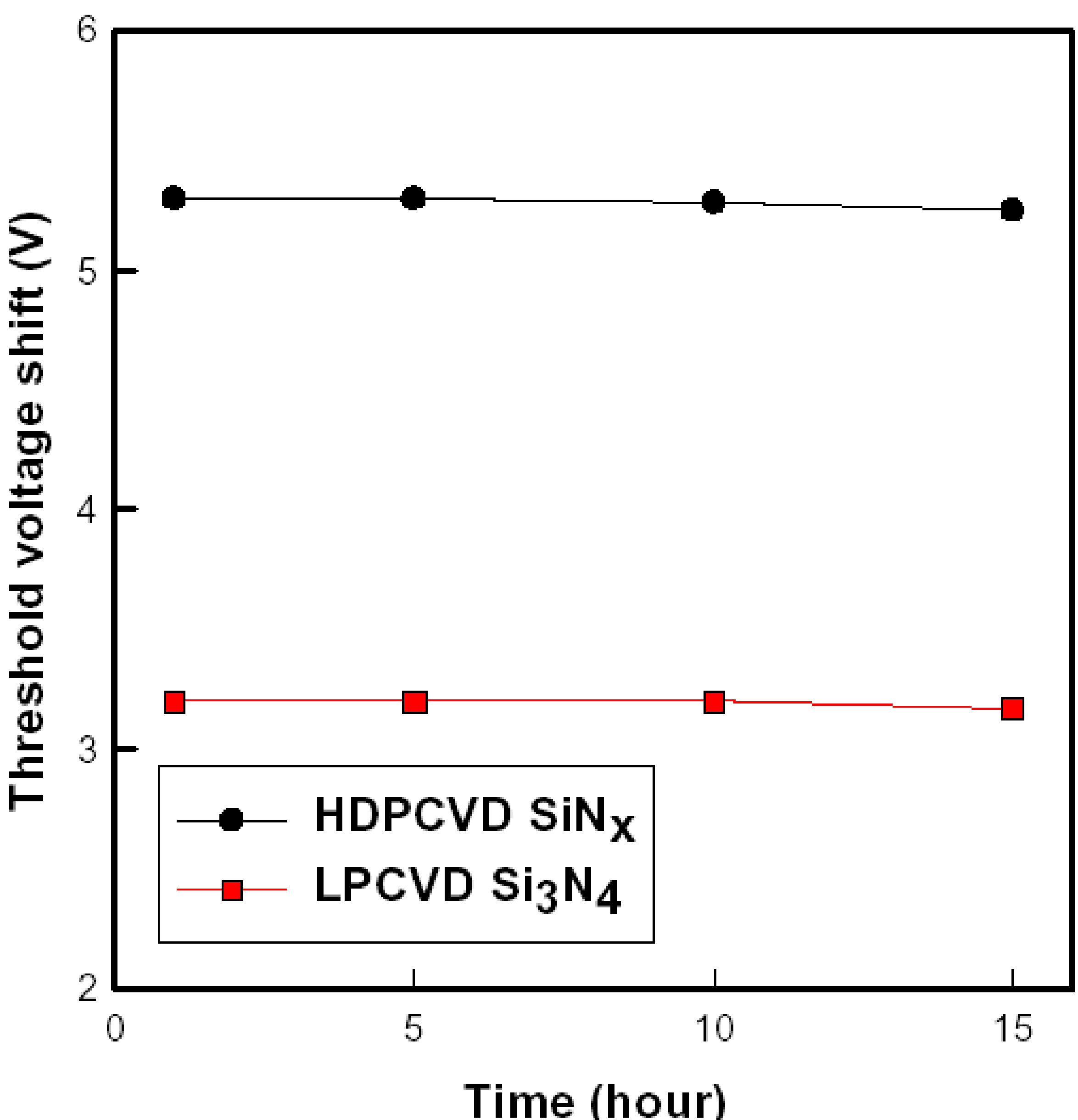




Si-N
N-H
HDPCVD SiNx
LPCVD Si3N4
Absorbance (A. U.)
Wavenumber(cm-1)
0.6
0.5
0.4
0.3
0.2
0.1
0.0
-0.1
-0.2
-0.3
500
1000
1500
2000
2500
3000
3500



SiO_2 / LPCVD Si_3N_4 / SiO_2
SiO_2 / HDPCVD SiN_X / SiO_2
Current density (A/cm^2)
Electric field (MV/cm)
10^{-7}
10^{-8}
10^{-9}
-4
-2
0
2
4

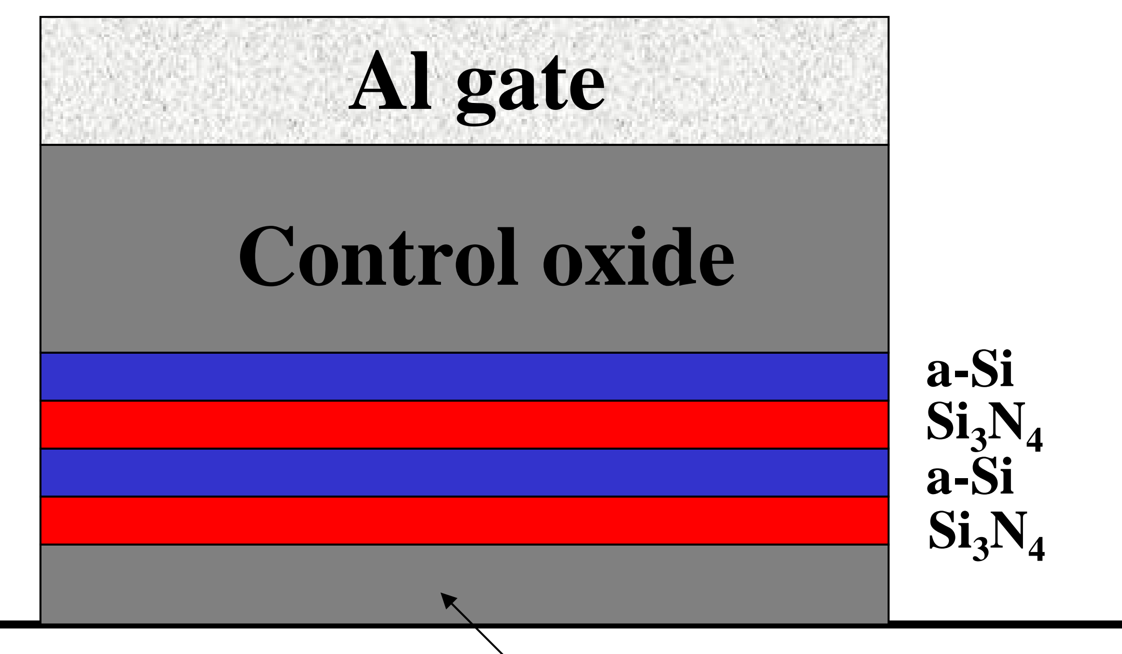


Threshold voltage shift (V)
6
5
4
3
2
0
5
10
15
Time (hour)
HDPCVD SiN_x
LPCVD Si_3N_4

Summary (5)

- HDPCVD SiN_x ONO stack, with a low leakage current, provides a larger memory window than the LPCVD Si_3N_4 ONO stack.
- With the optimization of the thickness in the gate-stacked ONO structure, the low-voltage and reliable operation, lower than 5V, is realizable.

Quasi-Superlattice Storage (QS^2): a novel concept of multilevel charge storage


Al gate
Control oxide
a-Si
Si_3N_4
a-Si
Si_3N_4
Tunnel oxide
Si substrate

Process Flow

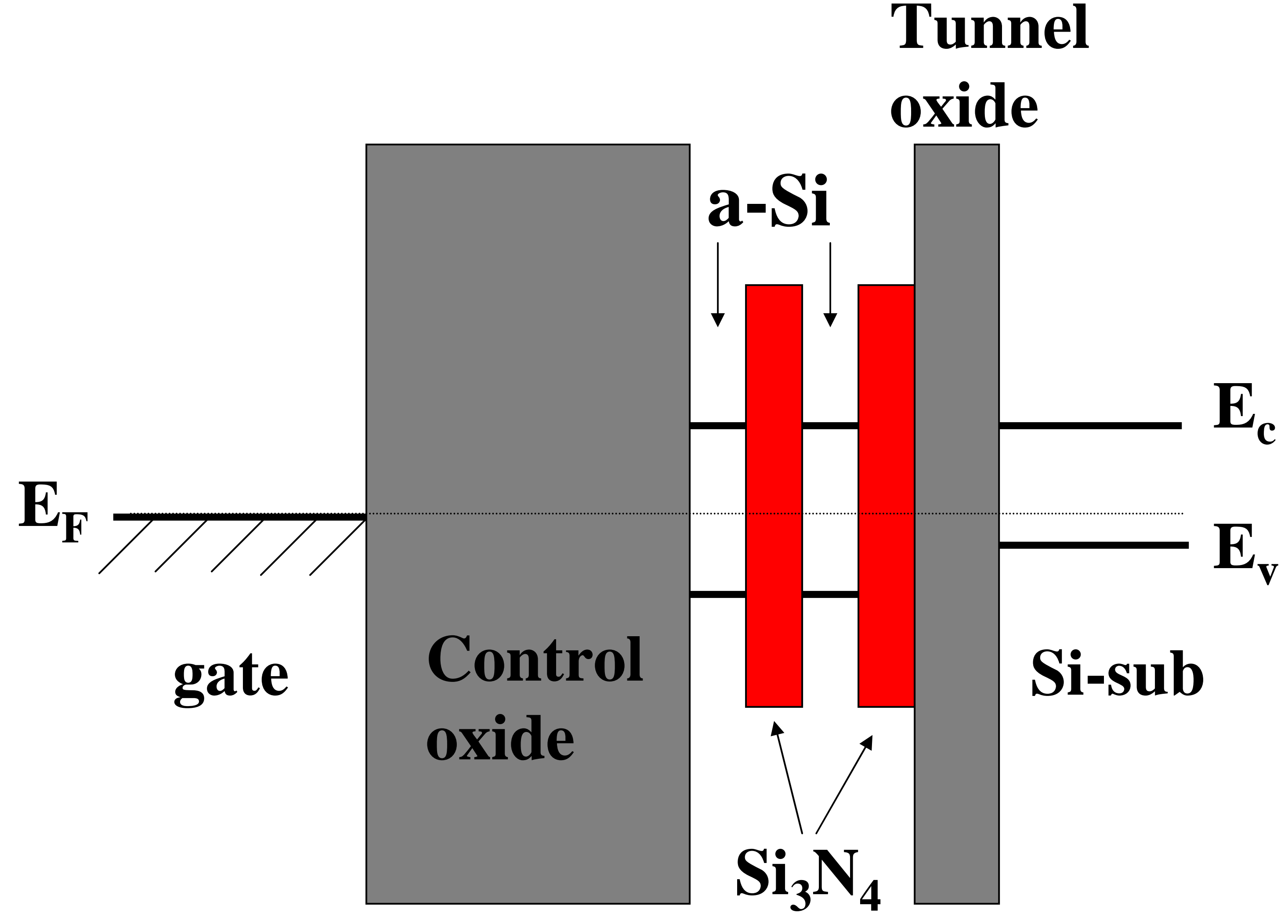
Standard clean → 3nm tunnel oxide growth → 2nm Si_3N_4 deposition →

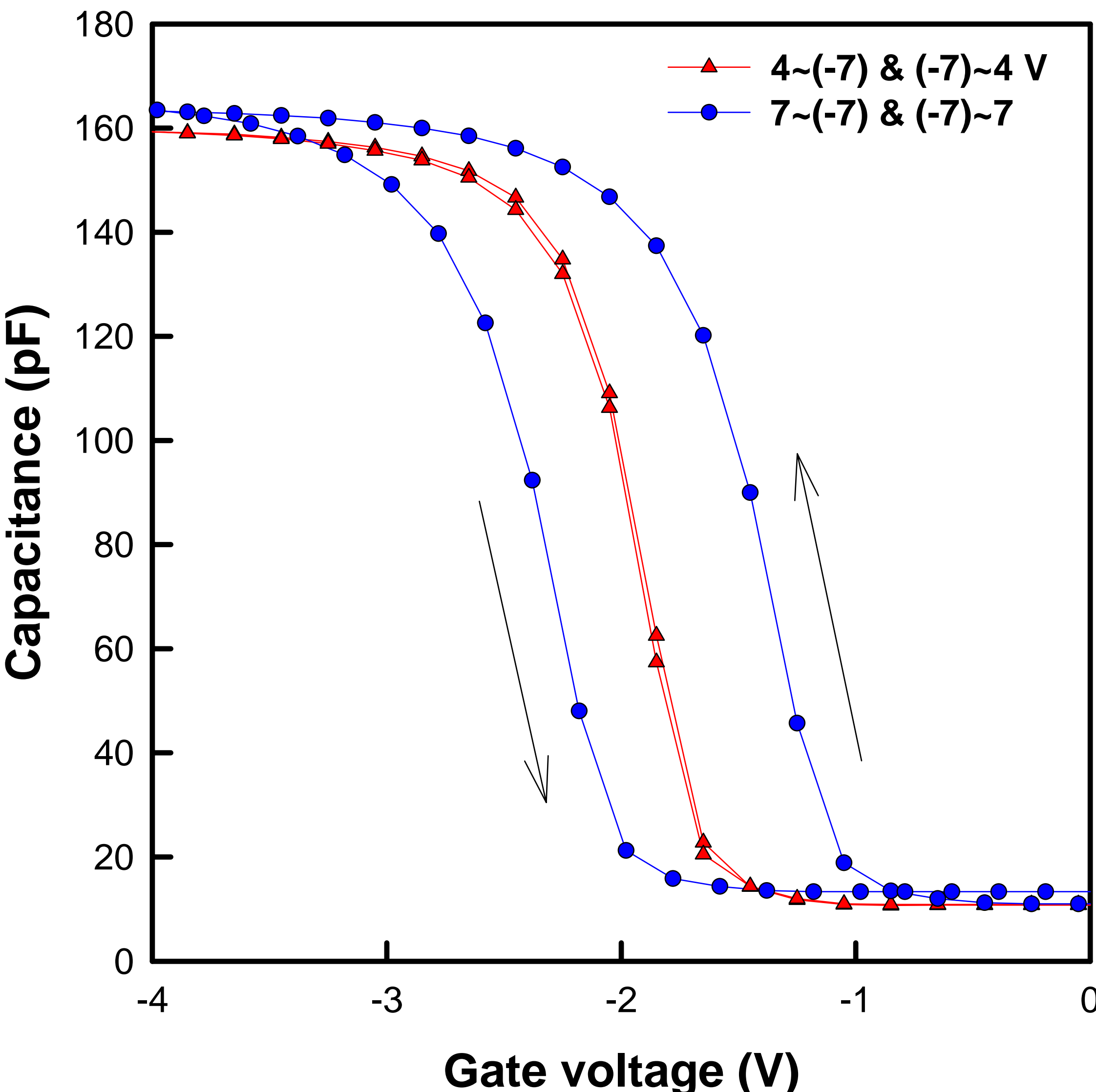
2nm a-Si deposition → 2nm Si_3N_4 deposition → 2nm a-Si deposition →

10nm TEOS oxide deposition → Steam densification at 982℃ for 180 sec → Backside etching →

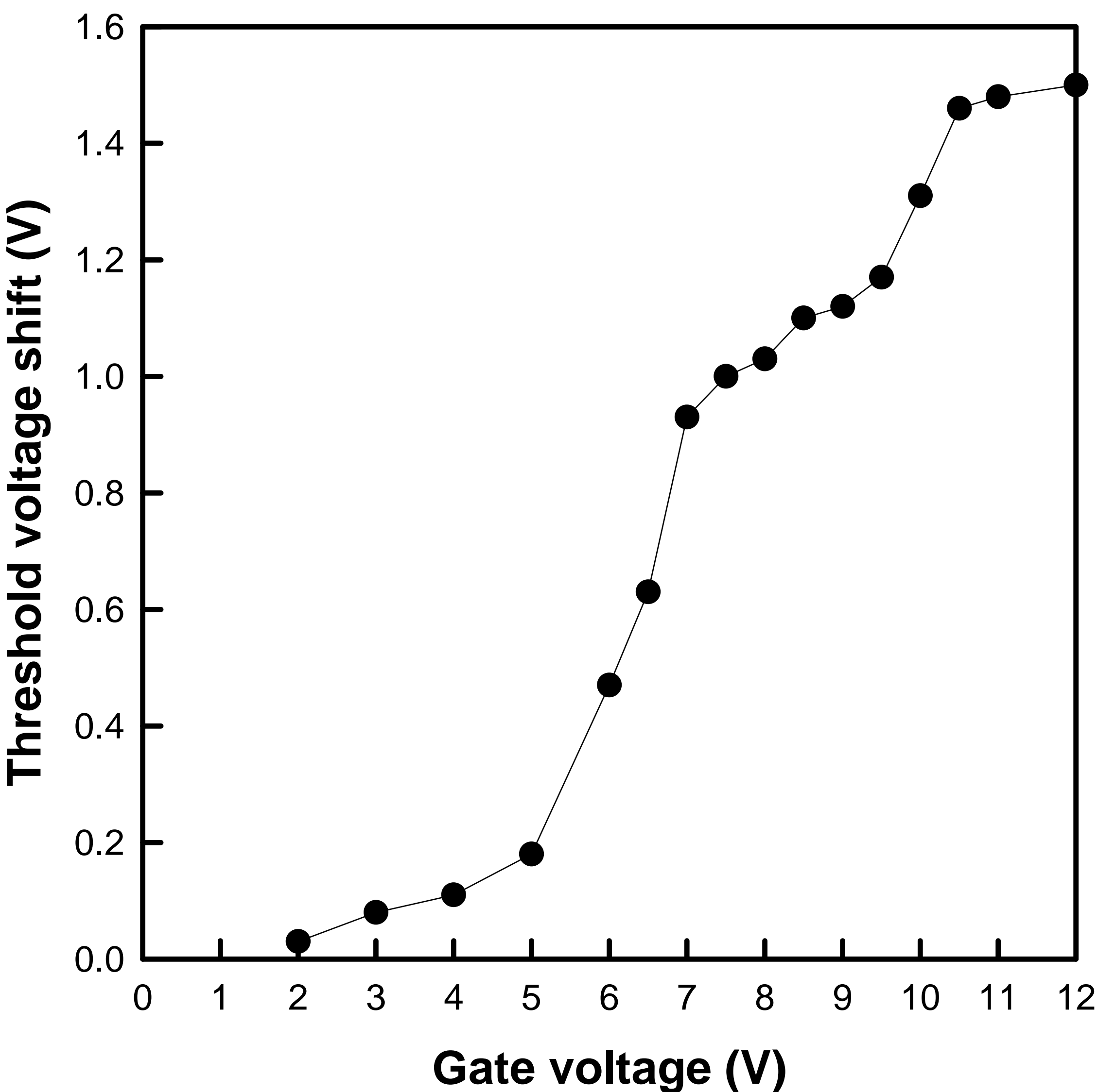
Electrode patterned, isolated and sintered → Electrical measurement

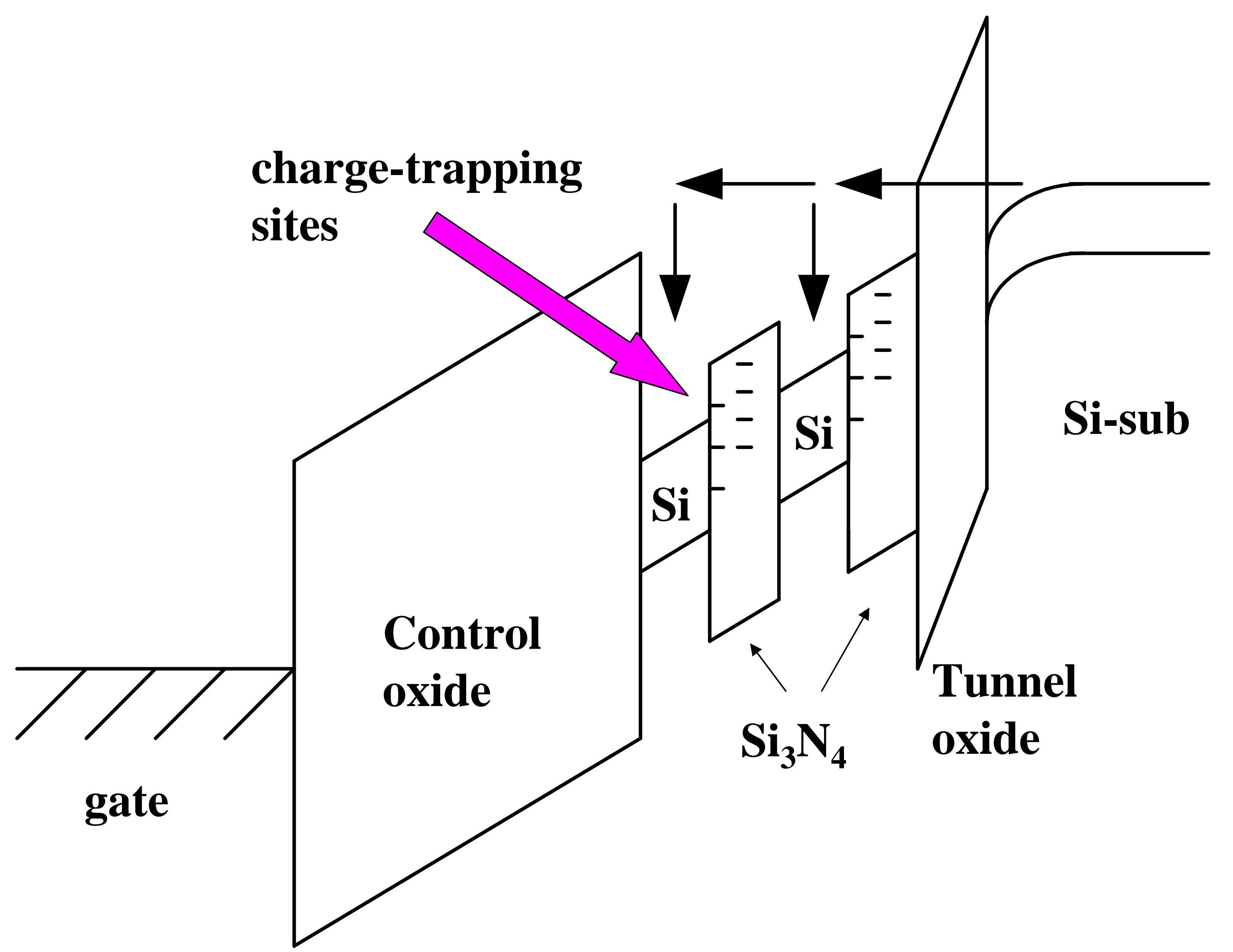
At V=0, the ideal energy band diagram



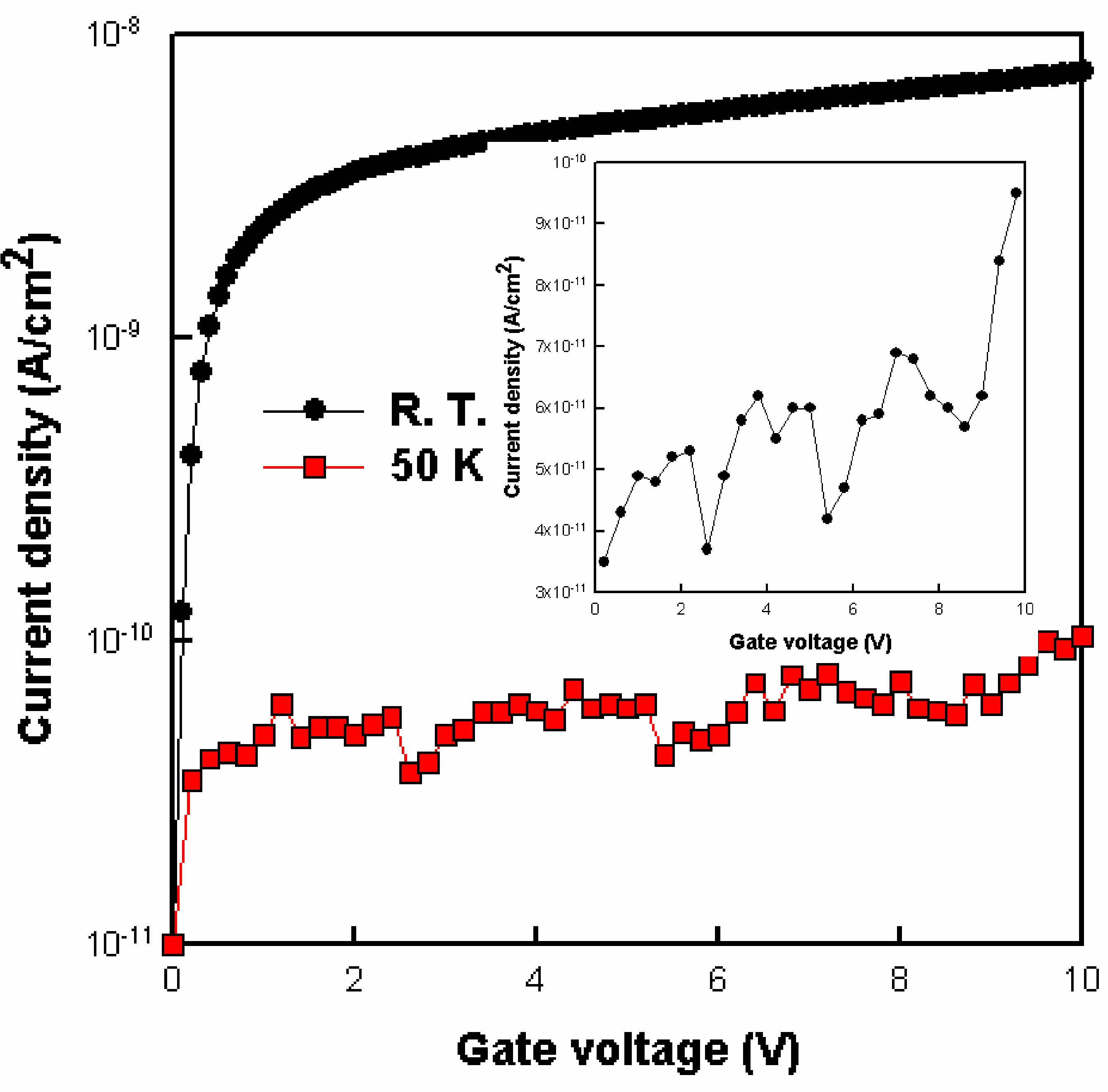


Capacitance (pF)
Gate voltage (V)
4~(-7) & (-7)~4 V
7~(-7) & (-7)~7
180
160
140
120
100
80
60
40
20
0
-4
-3
-2
-1
0

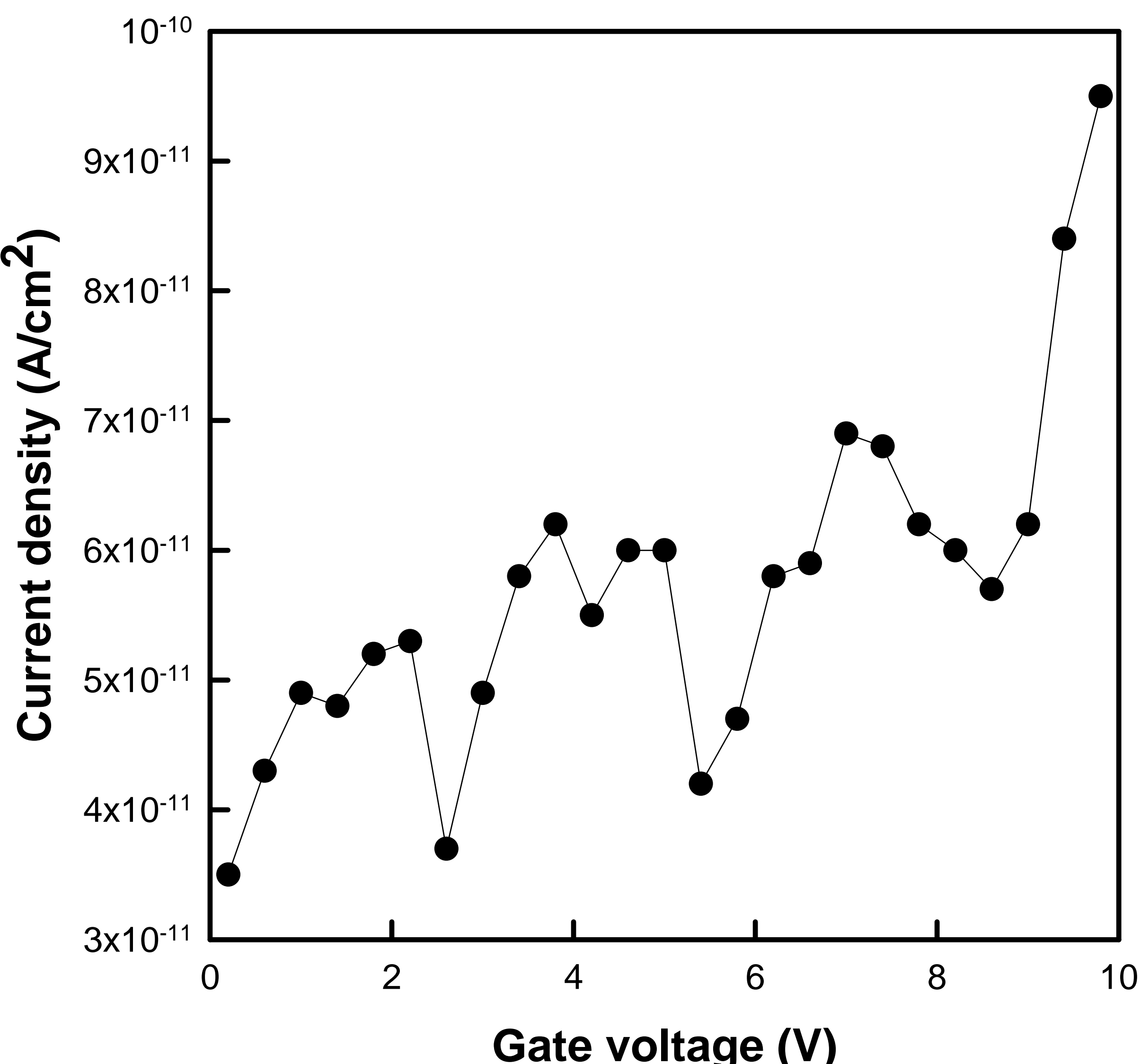

Threshold voltage shift (V)
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0
0
1
2
3
4
5
6
7
8
9
10
11
12
Gate voltage (V)


charge-trapping
sites
Si
Si
Si-sub
Control
oxide
Tunnel
oxide
Si_3N_4
gate

- The two sudden rises of the threshold voltage shift innovate the feasibility of 2-bit-per-cell operation under different operating voltages.
- For instance, memory state 1 can be defined at 6V and memory state 2 can be defined at 10 V.



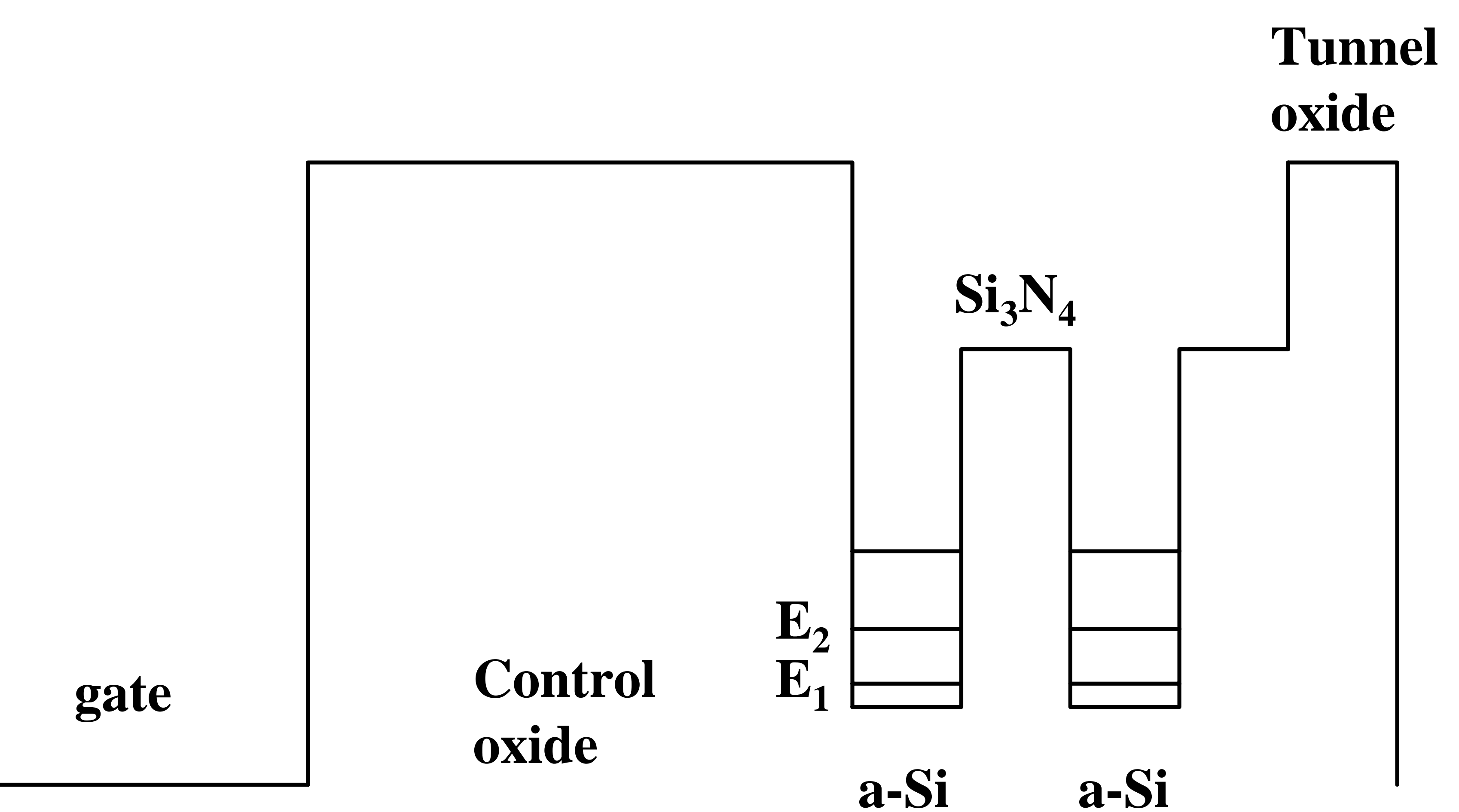
Current density (A/cm^2)
Gate voltage (V)
R. T.
50 K
10^{-8}
10^{-9}
10^{-10}
10^{-11}
0
2
4
6
8
10
Current density (A/cm^2)
Gate voltage (V)
10^{-10}
9×10^{-11}
8×10^{-11}
7×10^{-11}
6×10^{-11}
5×10^{-11}
4×10^{-11}
3×10^{-11}

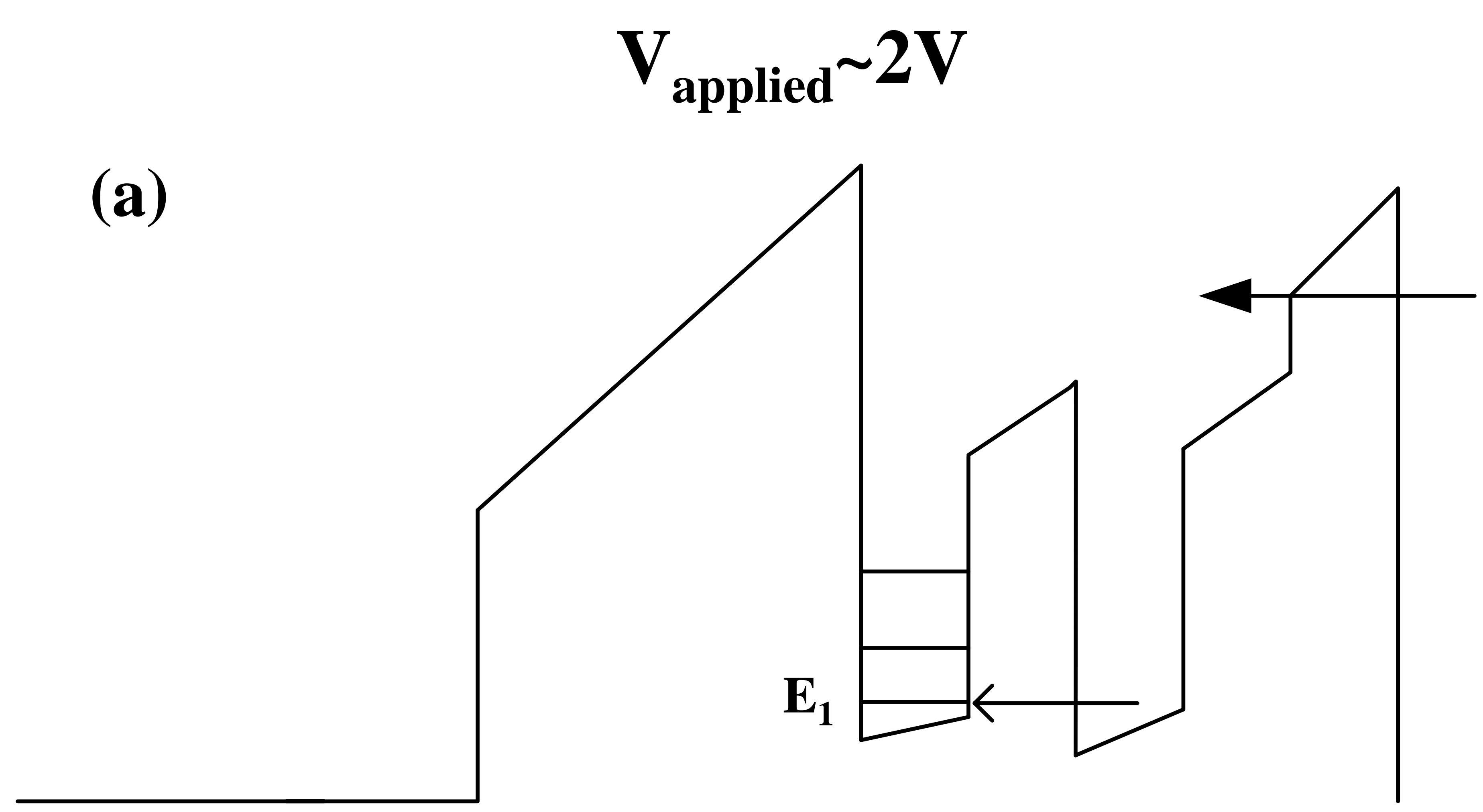


Current density (A/cm2)
Gate voltage (V)
10-10
9x10-11
8x10-11
7x10-11
6x10-11
5x10-11
4x10-11
3x10-11
0
2
4
6
8
10

- **The current-voltage characteristics behave like that of the resonant tunneling diode. The resonant tunneling is occurred at around 2V, 5.2V, 7V, and etc.**
- **Consider the resonant tunneling between the a-Si and nitride layers.**

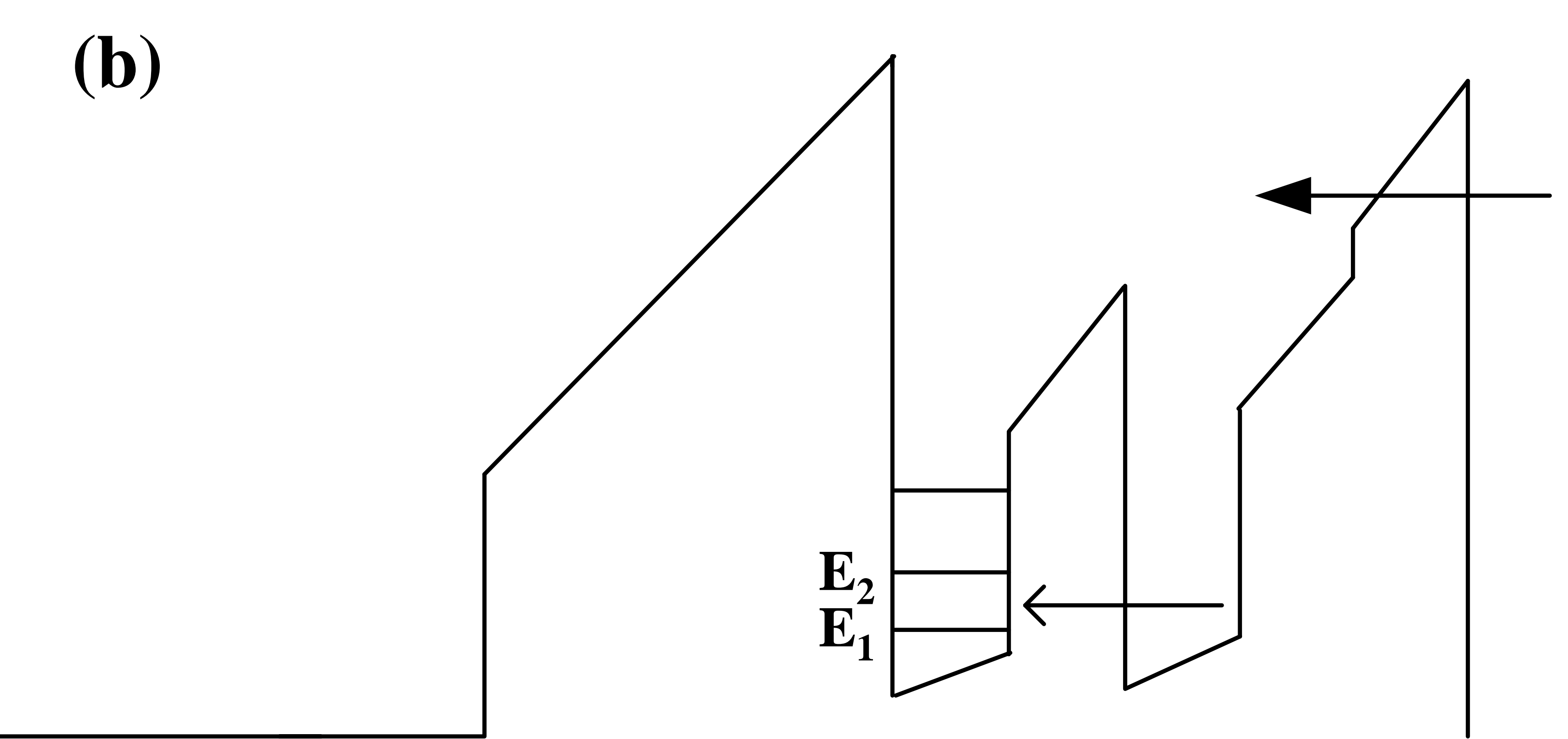
At V=0, the ideal energy band diagram



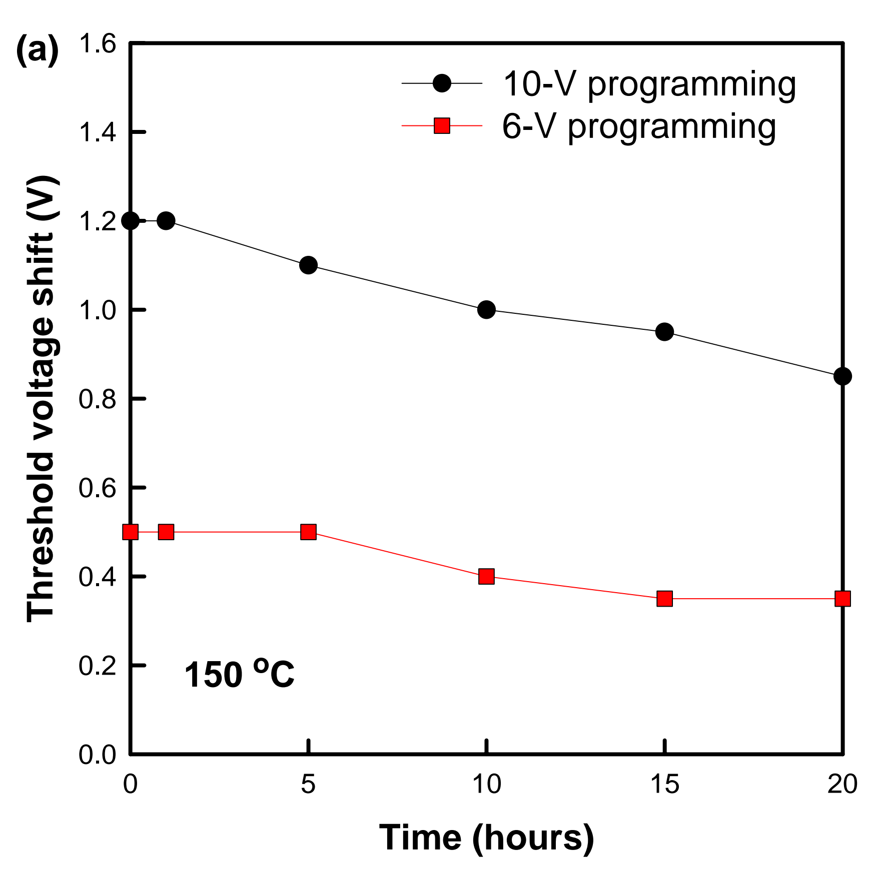


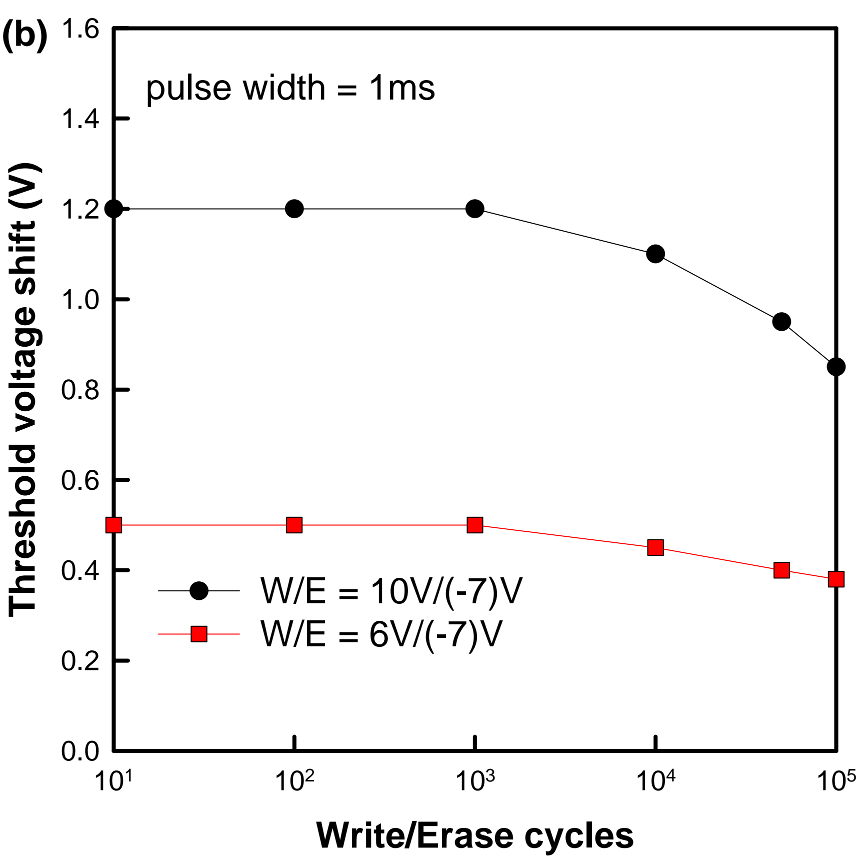
Vapplied~2V
(a)
E1

$2V < V_{applied} < 5.2V$



Retention and endurance characteristics of the quasi-superlattice memory device





Summary (6)

- The quasi-superlattice structure provides the possibility and viability of 2-bit-per-cell operation.
- A physical model is proposed to explain the multilevel charge storage of the QS structure.
- The negative differential resistance occurs at low temperature in a manner of resonant-tunneling-diode-like (RTD-like) leakage behavior.

Conclusion

- To stimulate the nonvolatile memory devices move into a faster and smaller regime, the tunnel oxide thickness needs to be shrunk.
- Optimization of ONO stack and new storage materials are widely pursued in SONOS nonvolatile memory technology.

Conclusion (cont.)

- The uniformity of the nanocrystals, size and size distribution, determines the key to the mass production of nanocrystal nonvolatile memory devices.
- The advanced nonvolatile memory devices with tunnel oxide less than 7 nm deserve more attention on the study of retention, endurance, disturb, retention after stress, and etc.

T. C. Chang et al., Electrochemical and Solid-State Letters, **7**(1), p. G17 (2004)

T. C. Chang et al., Applied Physics Letter, **84**(12), p.2094 (2004).

T. C. Chang et al., Applied Physics Letter, **84**(14), p.2581 (2004).

T. C. Chang et al., Applied Physics Letter, **84**(18), p.3687 (2004).

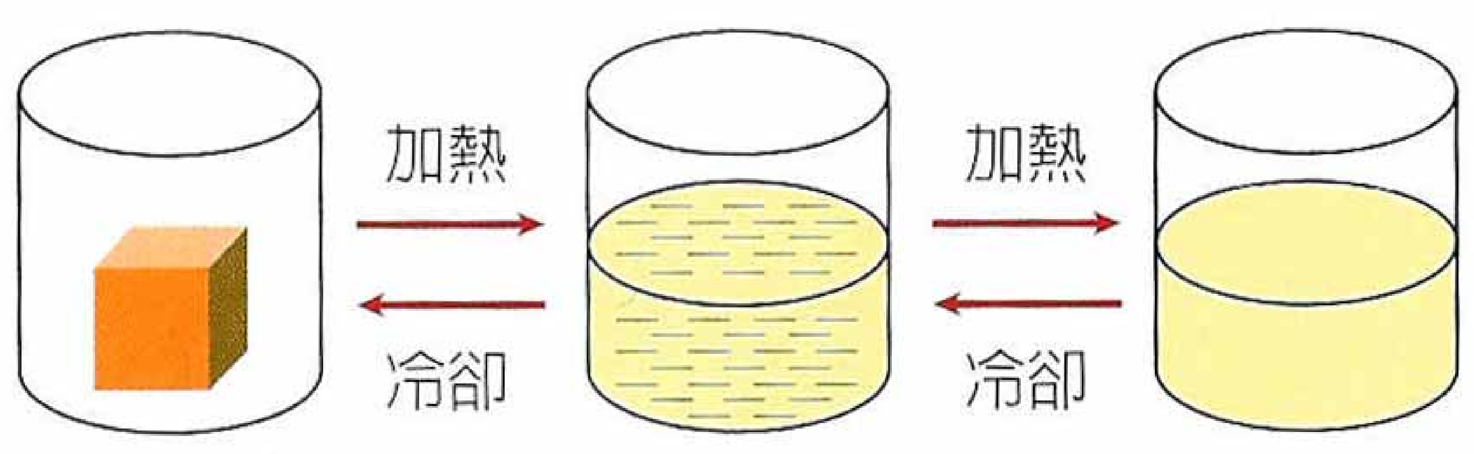
T. C. Chang et al., Applied Physics Letter, **85**(2), p.248 (2004).

奈米線薄膜電晶體(nano wire -TFT)在平面顯示器之應用與研究

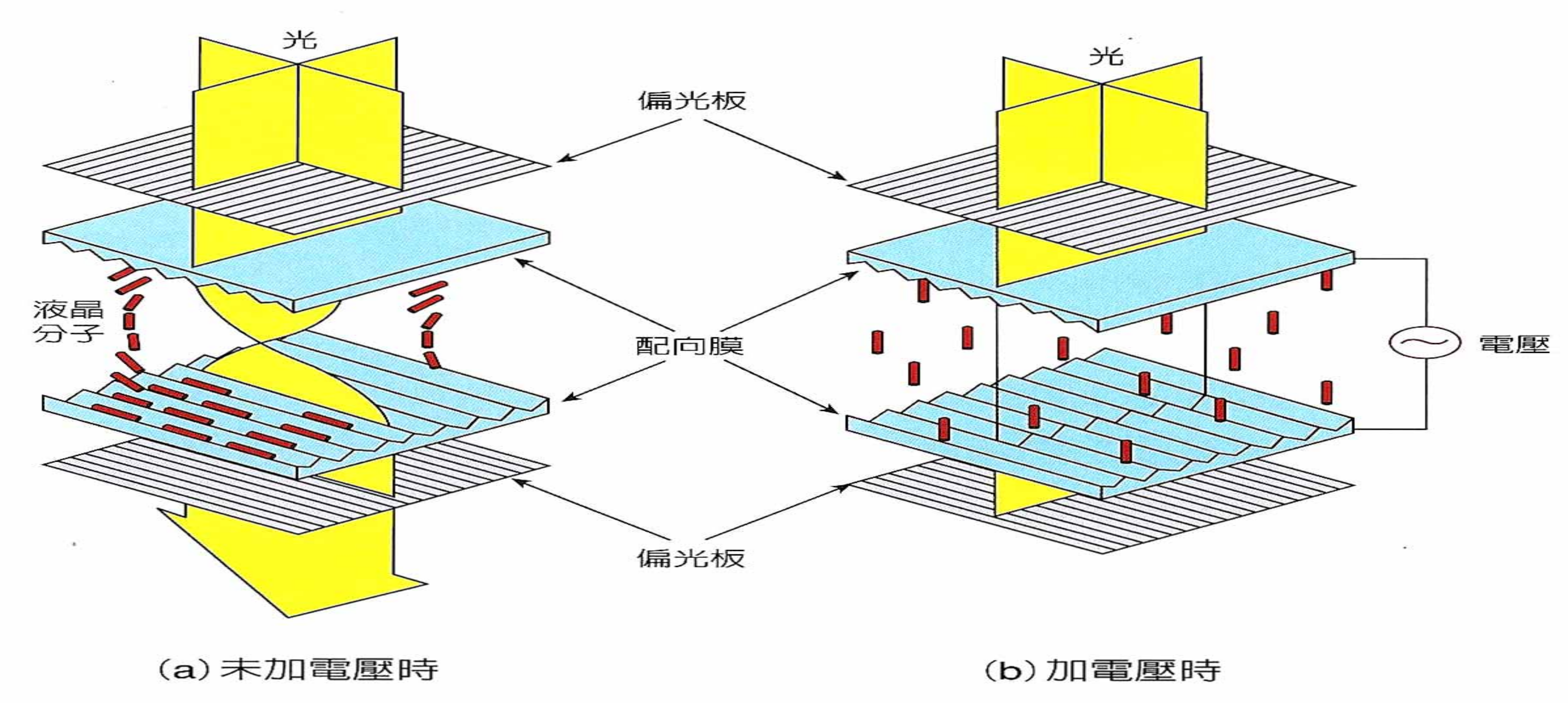
"High performance polycrystalline silicon thin film transistor with multiple nano-wire channels and LDD structure"
Applied Physics Letter, 84(19), p.3822 (2004)

内建無線數據機的手機，可提供高速數據128000位元／秒傳輸；使用手機通話的同時，可以看到對方的臉，所有的動作表情盡收眼底。

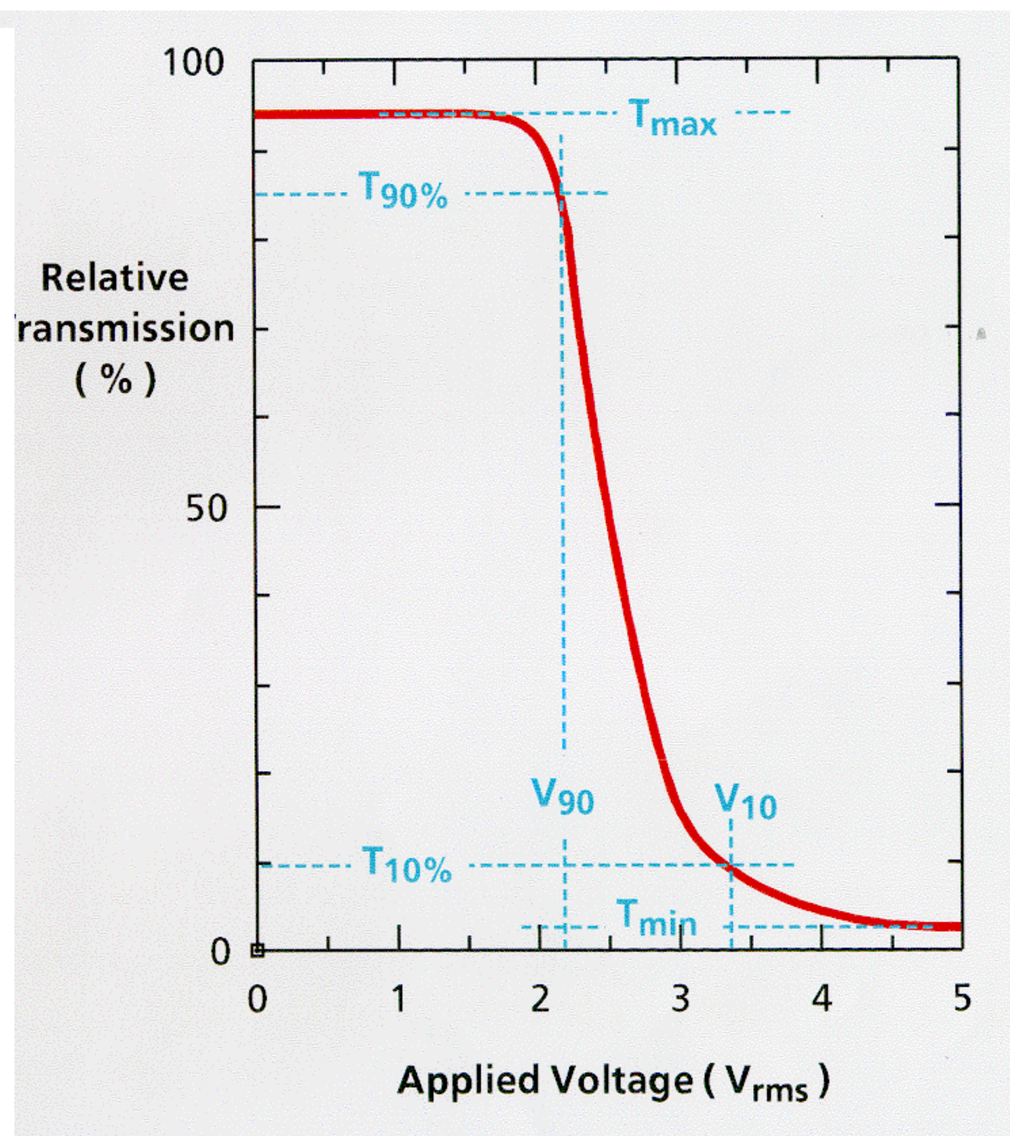
- 液晶特性



同時具有晶體規則性與液體流動性的液晶會因溫度的增加或下降變化，而造成液晶狀態的改變。



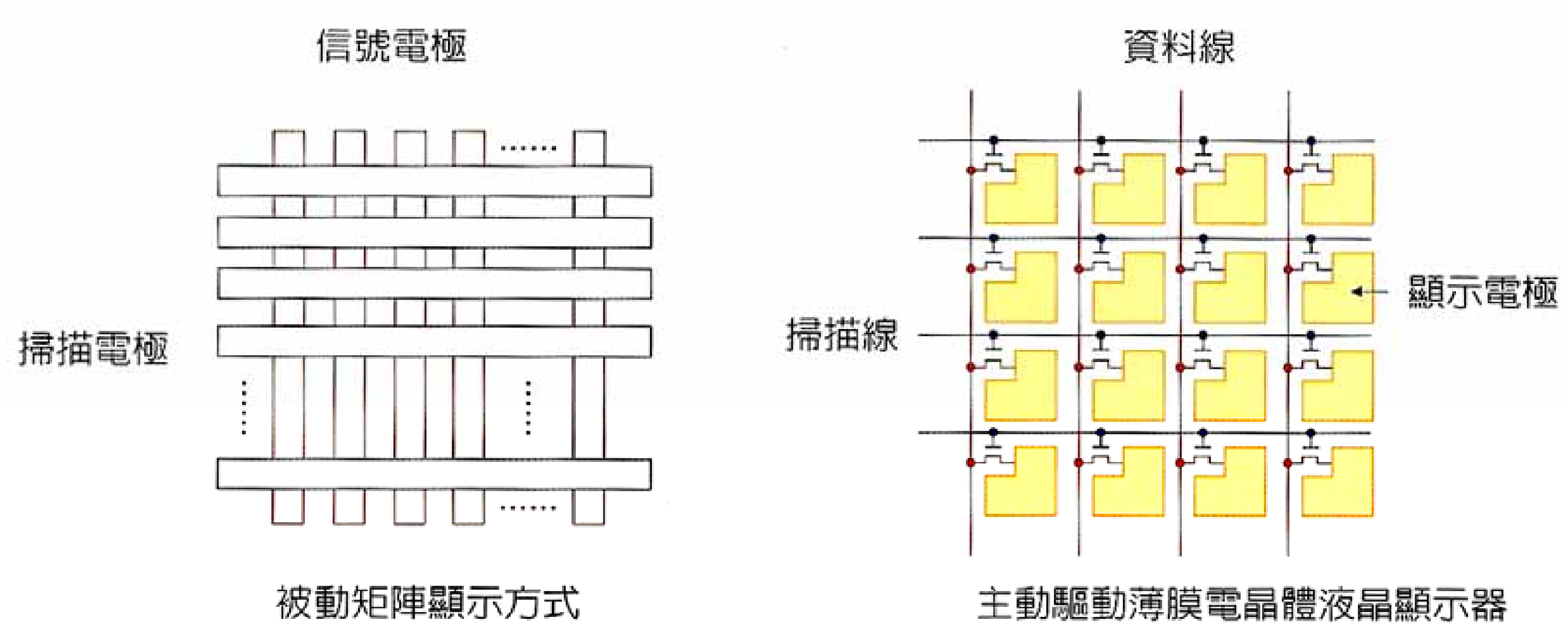
扭轉向列型液晶顯示器之工作原理；利用外加電壓來改變液晶分子排列狀態，進而達到亮暗對比的顯示效果。



- Contrast ratio = T_{max} / T_{min}
- Grey scale achieved with intermediate values of V_{rms}

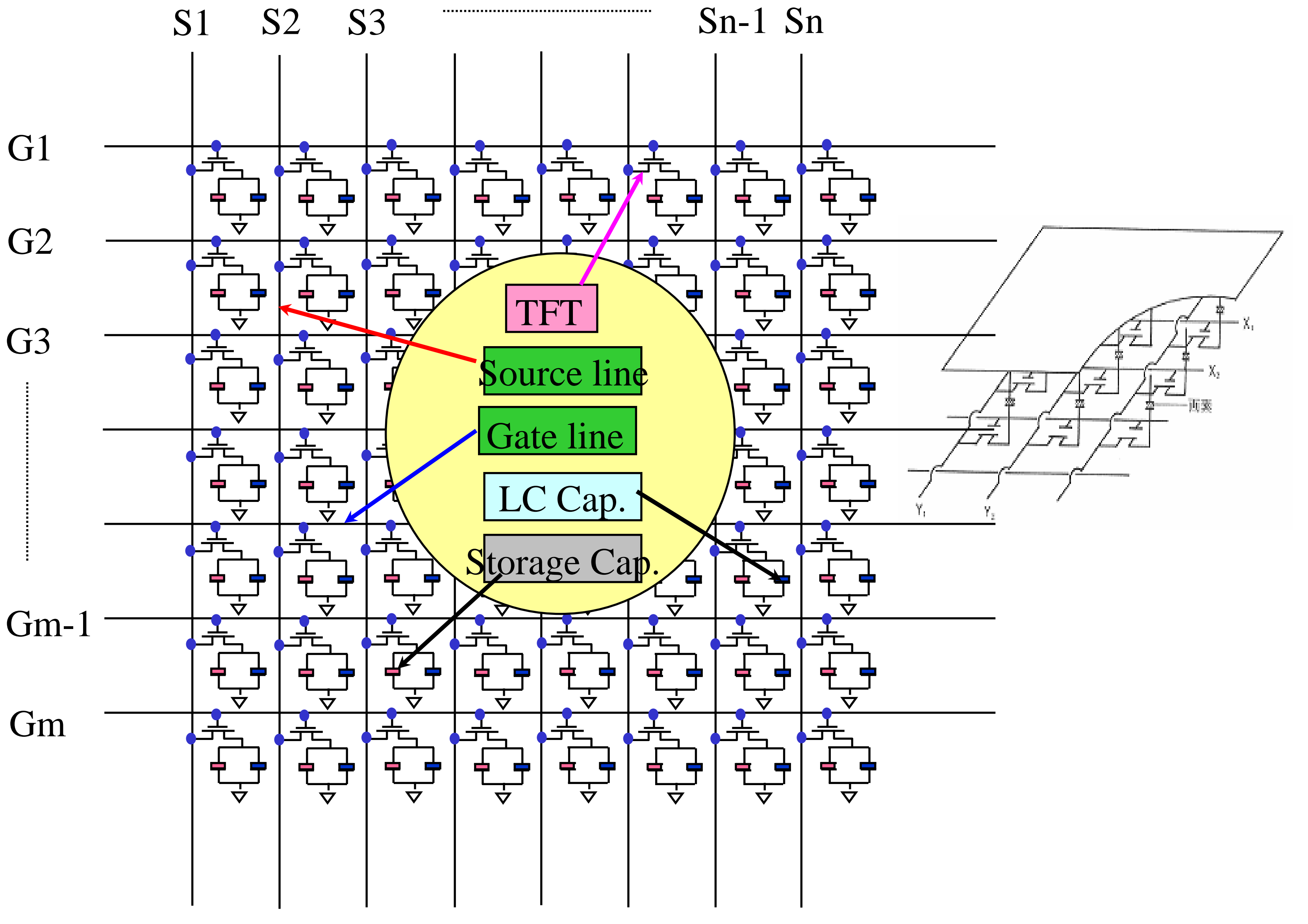
6-bit => 64 voltage levels
(262,000 colors)

8-bit => 256 voltage levels
(16.7 million colors)

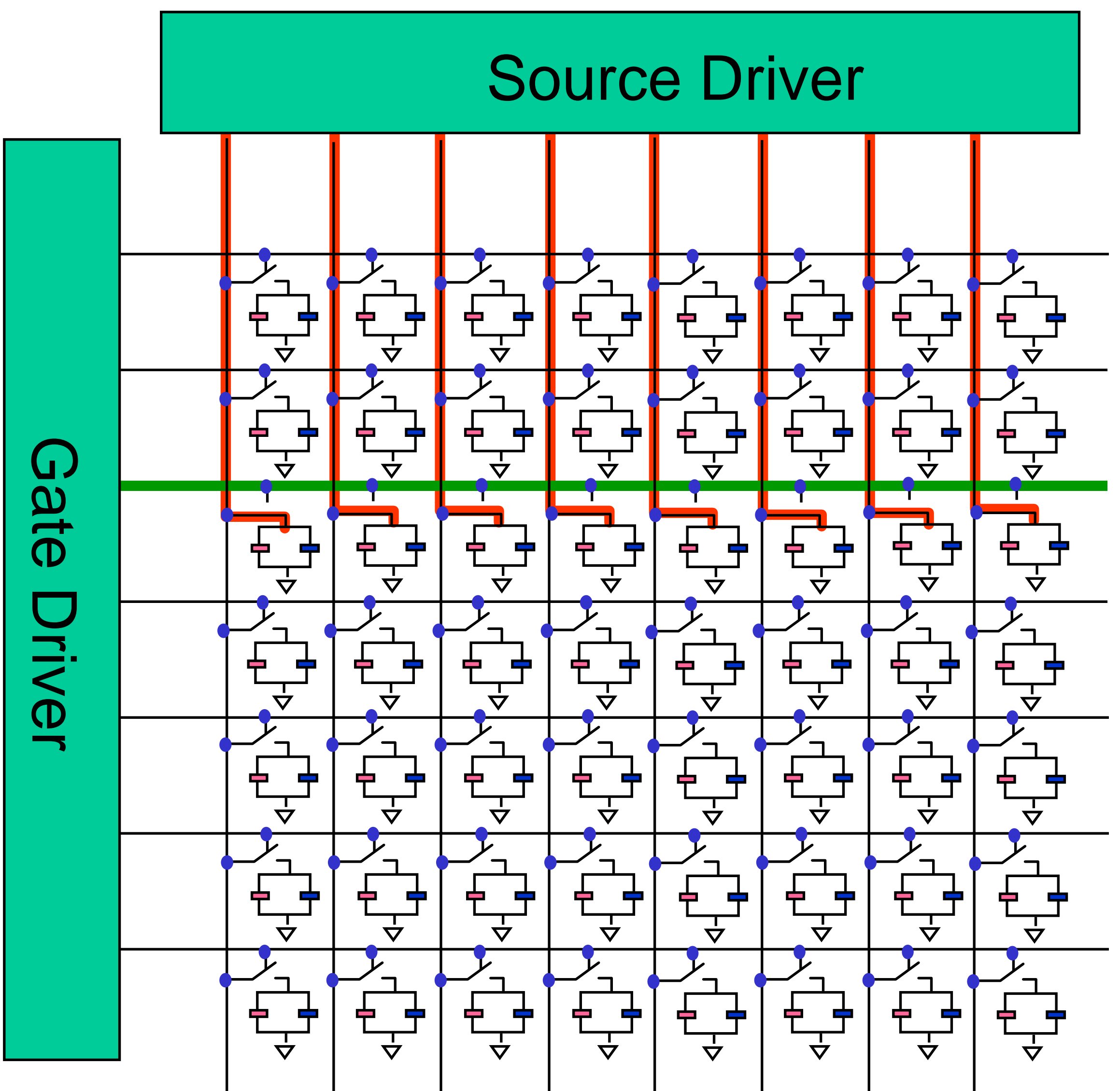


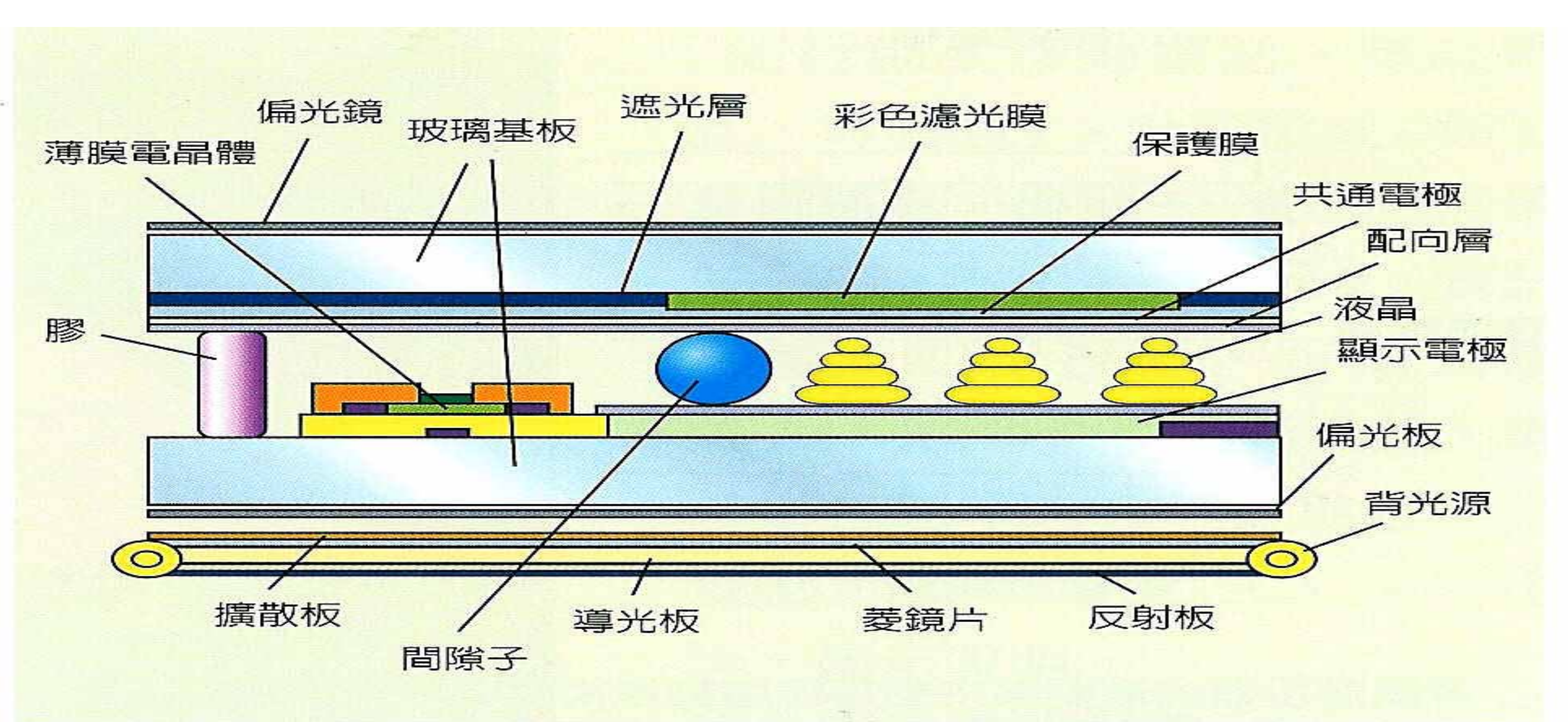
液晶顯示器的被動與主動矩陣驅動技術：利用掃描電極與資料電極的安排來達到點矩陣的驅動形式，而主動驅動液晶顯示器是運用主動元件（如電晶體）來控制各畫素的開關 。

TFT-LCD Operating Principle



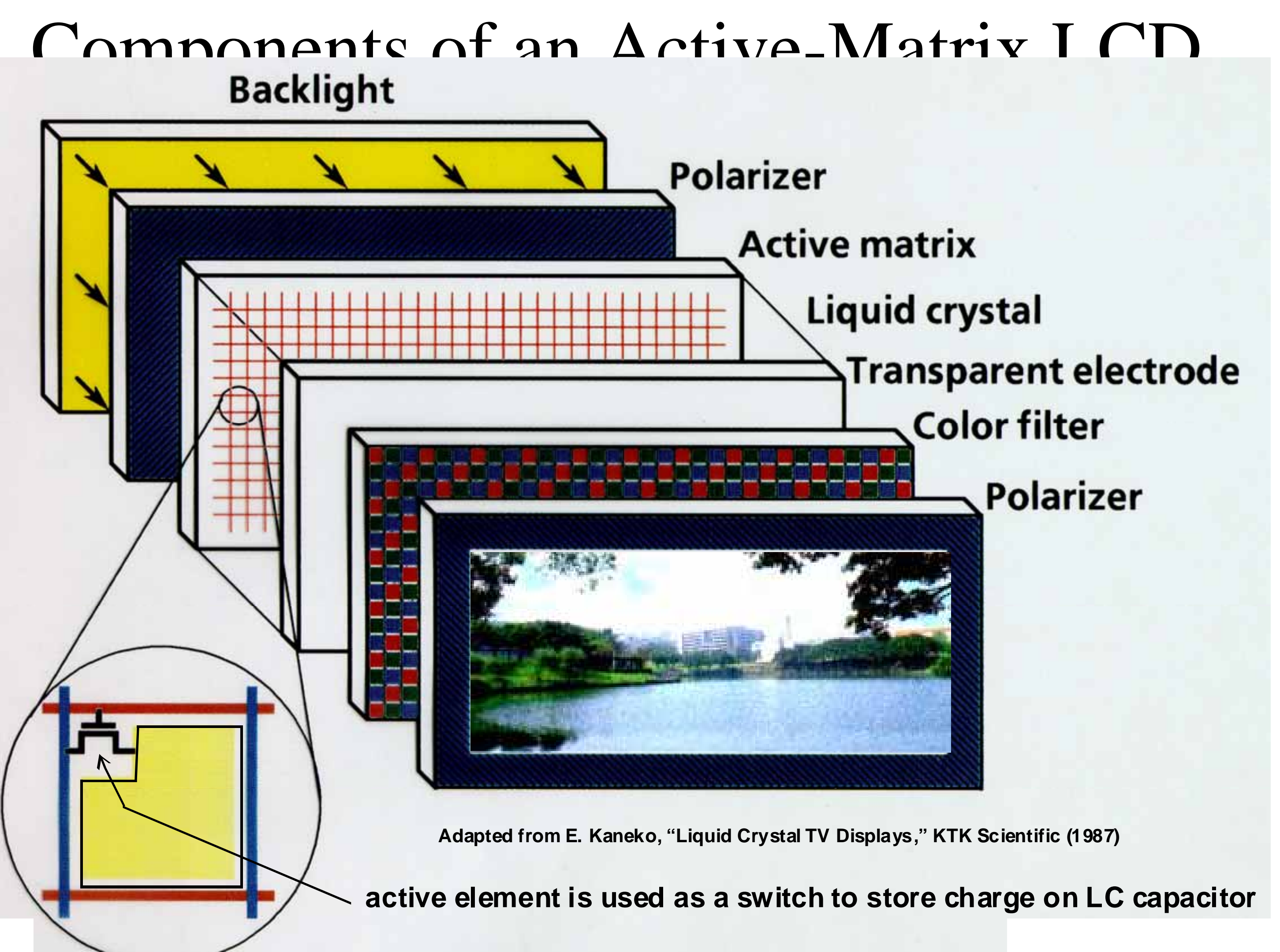
TFT-LCD Signal Driving





薄膜電晶體液晶顯示器的結構示意圖，在兩片玻璃基板間夾有一定排列方向的液晶分子層，利用間隙子控制液晶盒的均勻厚度。

Components of an Active-Matrix LCD

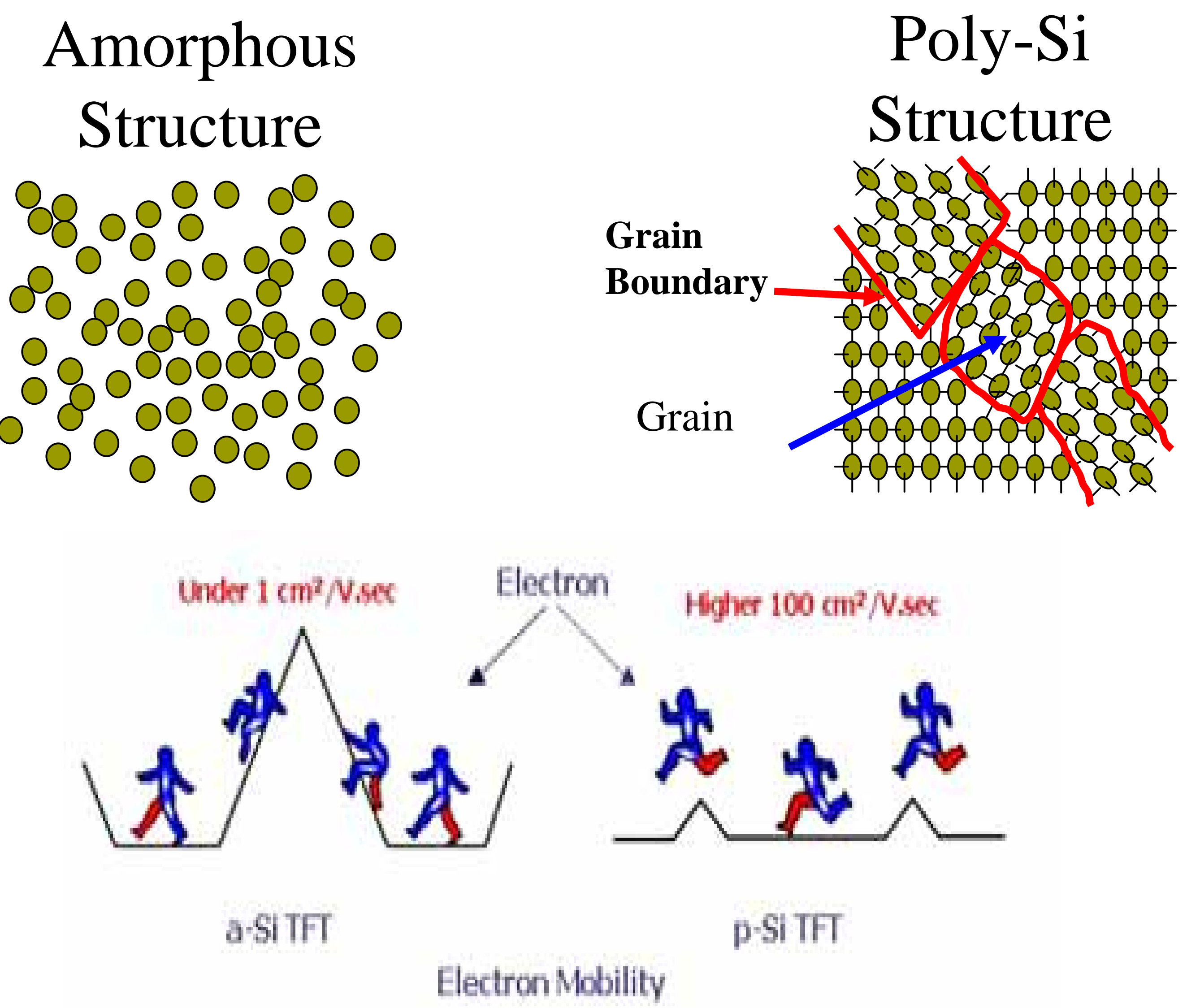


Adapted from E. Kaneko, "Liquid Crystal TV Displays," KTK Scientific (1987)

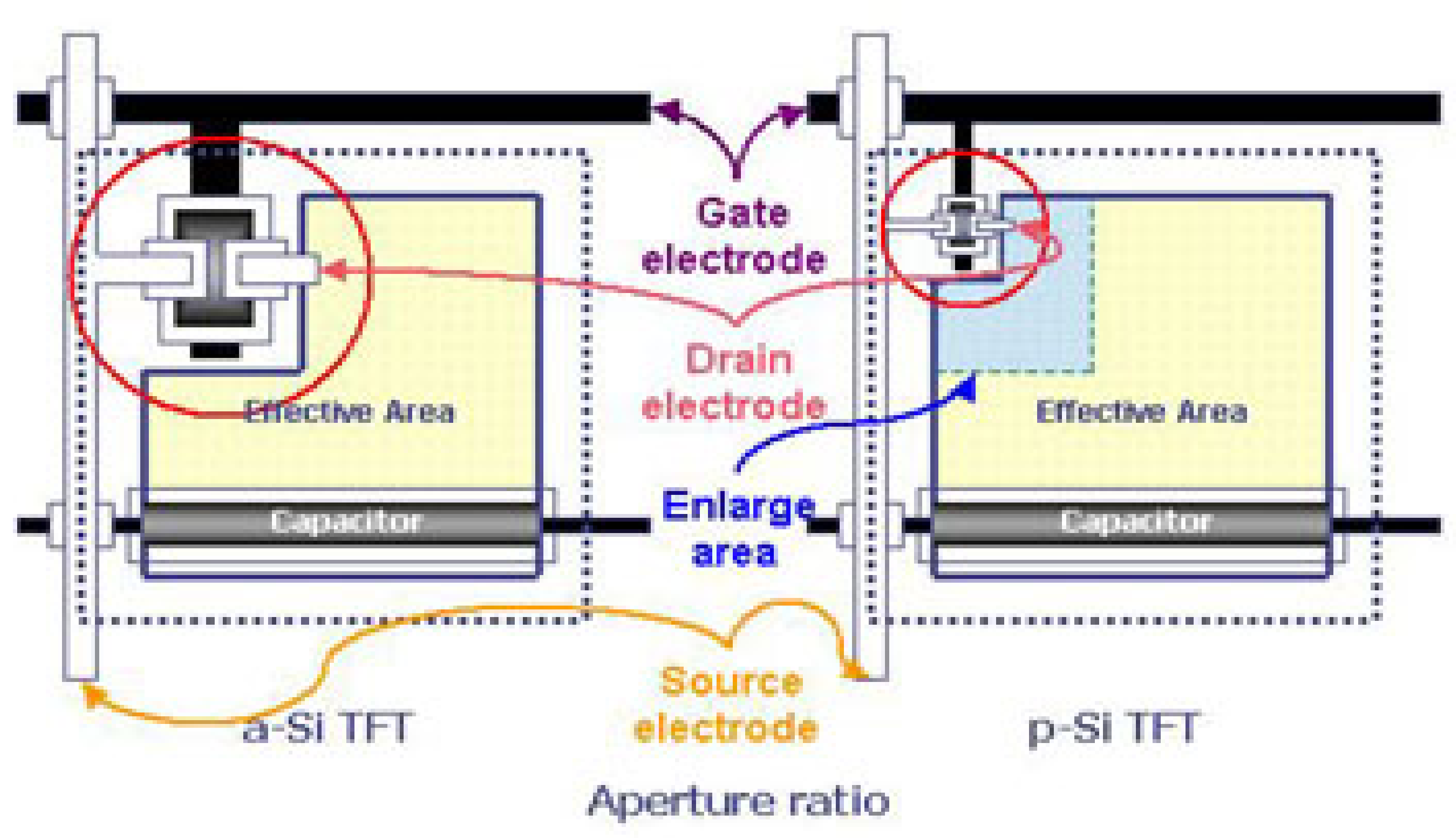
Silicon Thin Films -- Classification

	a-Si amorphous	poly-Si poly-crystal	c-Si single crystal
Field Effect Mobility μ (cm^2/Vs)	0.5 - 1.0	30 - 300	600 - 700
Crystal Structure	Short range order H-termination	Grain boundary	Perfect
Application	Pixel Switching	Driver Circuit	Driver LSI

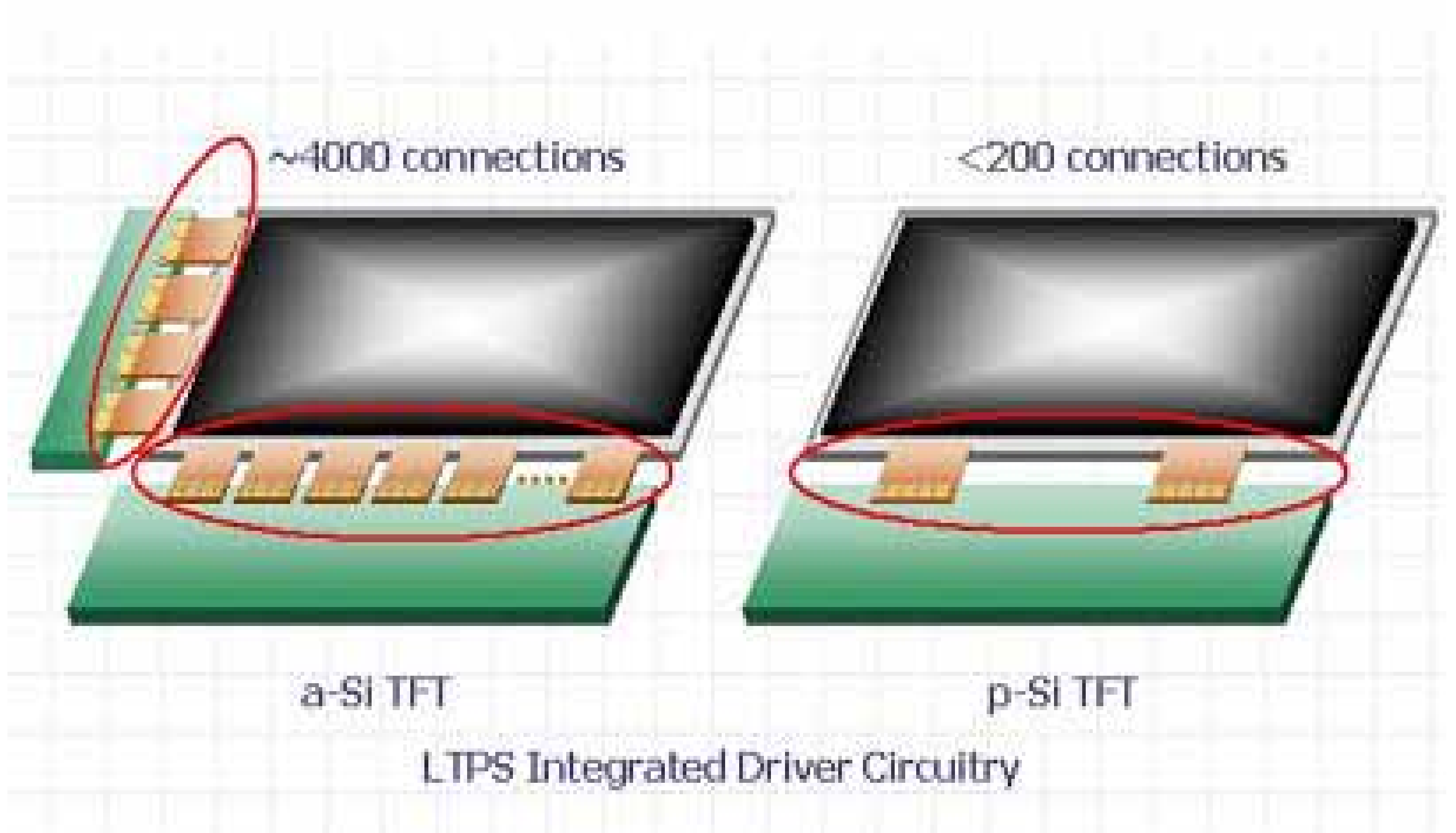
- **Silicon thin film**



● Aperture Ratio in a-Si and p-Si TFTs

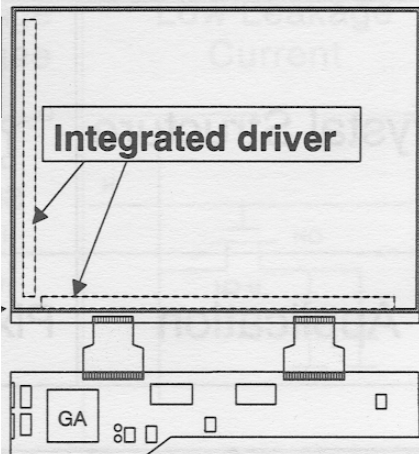


● Reliability in a-Si and p-Si TFTs

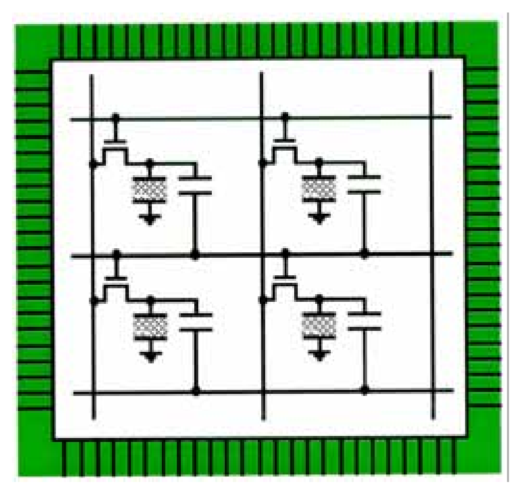


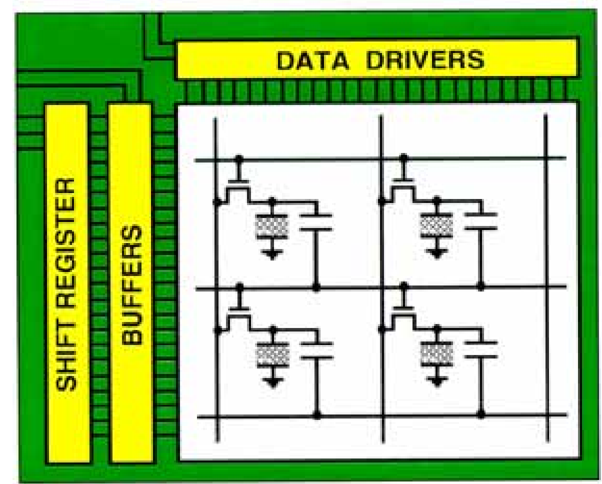
Advantages of Poly-Si TFT Technology

- Higher pixel aperture ratio
  → higher brightness, or lower power displays
- Higher resolution
  - not limited by TAB-IC connection pitch
- More compact and reliable display module
  - ~95% fewer external connections (“3 sides free”)
  - reduced number of electronic components



TFT Technology Comparison





AMORPHOUS SILICON

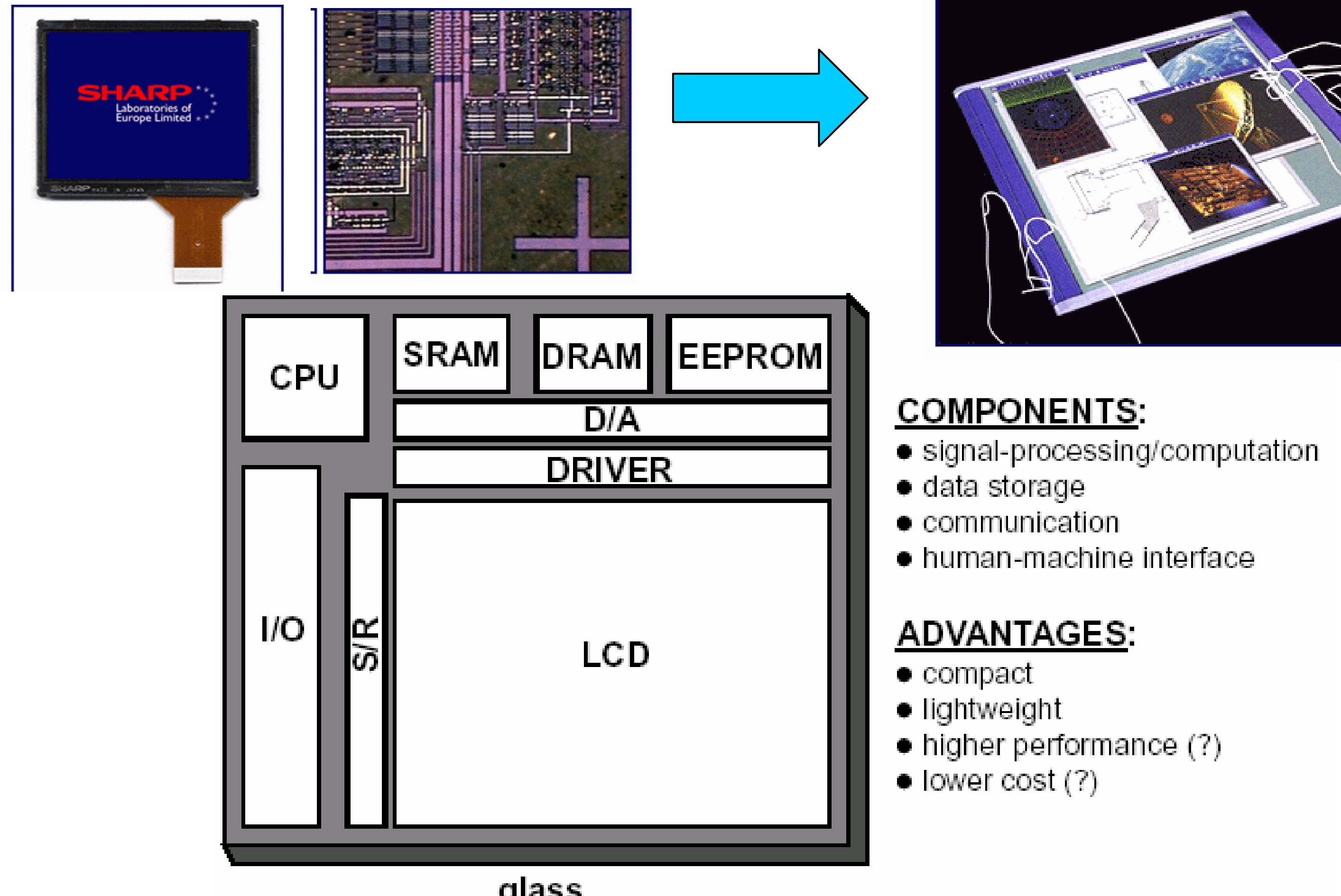
- low carrier mobility (μ_n<1 $cm^2/V \bullet s$)
  → separate IC drivers needed
  (TAB-IC pitch limited to ~150 ppi)
- low-temperature (<350°C) process
  → low-cost glass substrates

POLYCRYSTALLINE SILICON

- higher mobilities (μ_n, μ_p>30 $cm^2/V \bullet s$)
  → smaller pixel TFTs
  → integration of driver circuitry
- high-temperature (>450°C) process
  → high-strain-point glass or quartz substrates

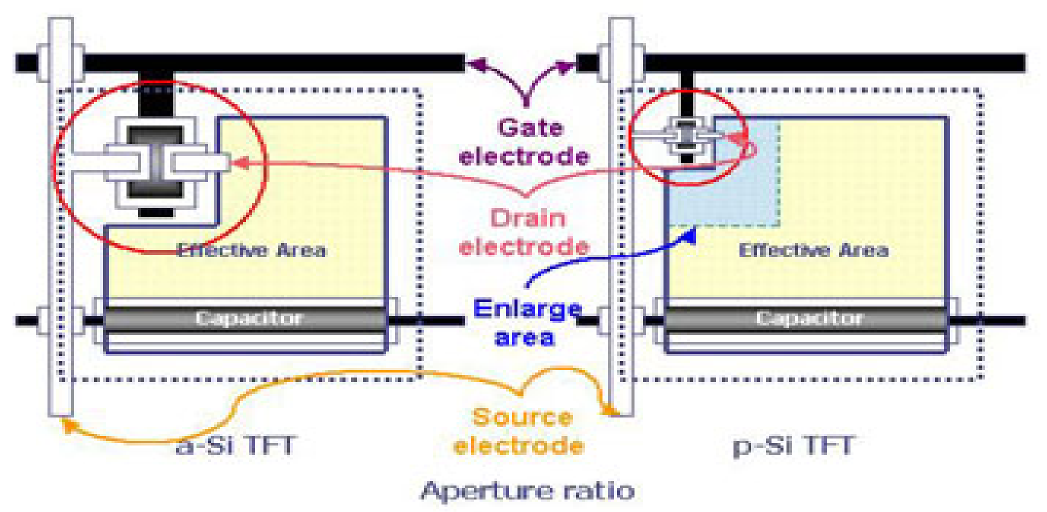
LTPS TFT-LCDs

LTPS display with integrated driver **System on panel**



- **Advantage of using poly-Si TFTs**

1. Larger aperture ratio
2. Higher circuit density
3. Larger driving current
4. Apply to AMOLED
5. Realization of System on Panel

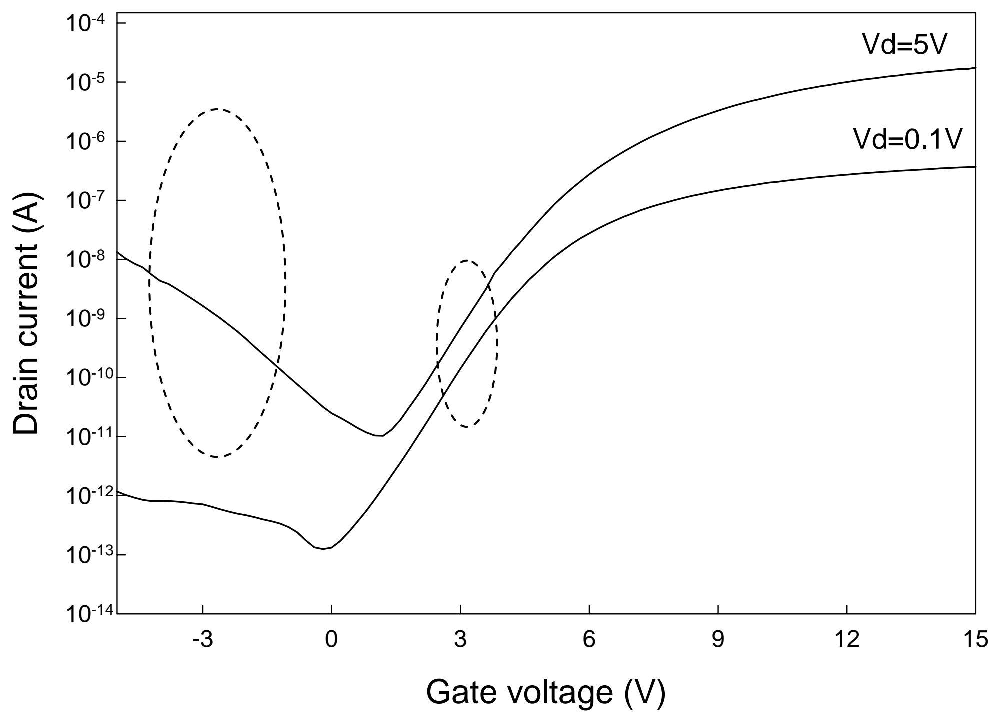


Driving current

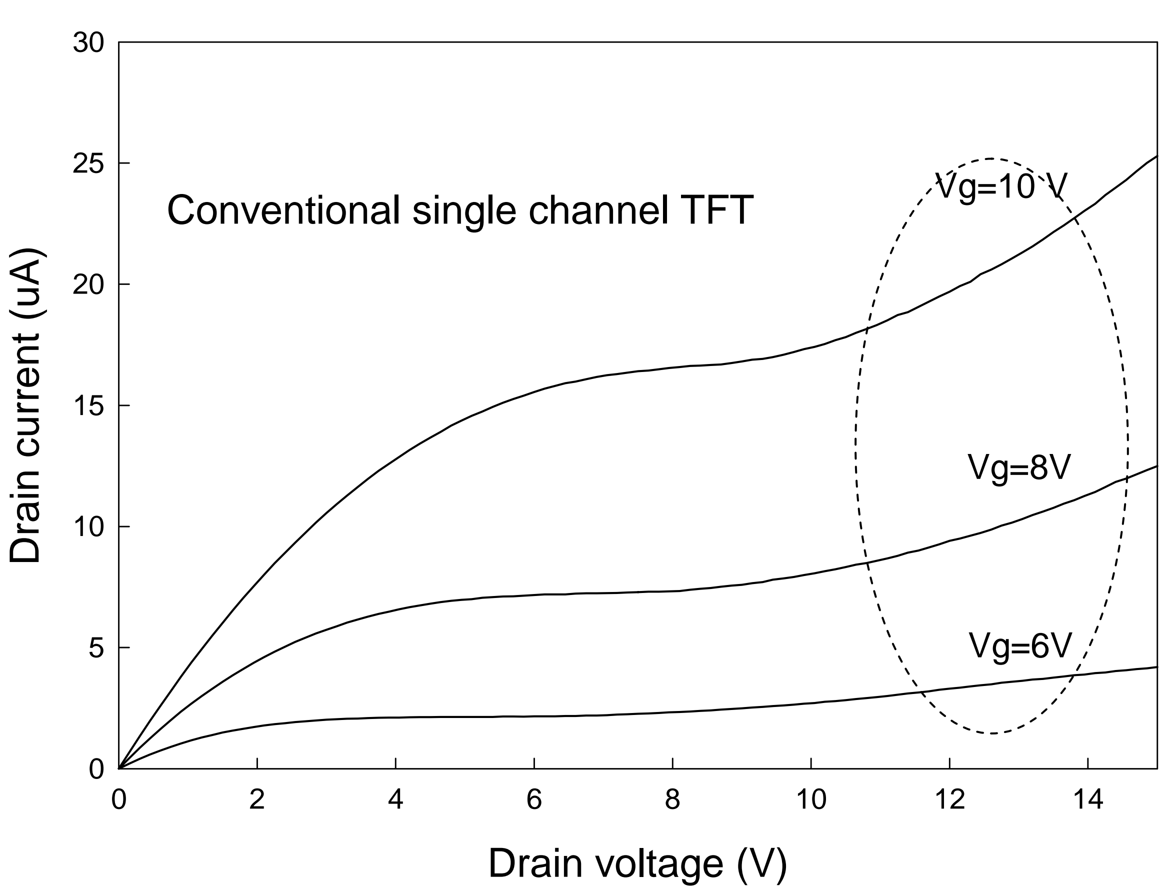
$$I_D \propto \mu \frac{W}{L}$$

- **As the channel scaling**

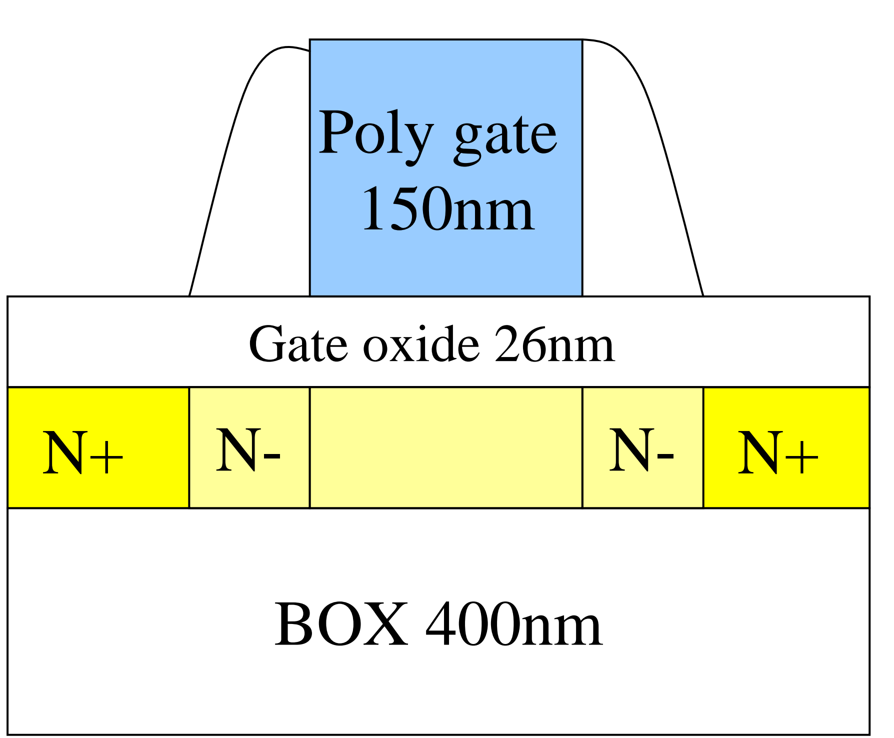
1. Leakage current
2. Drain induced barrier lowering (DIBL)



3. Kink effect

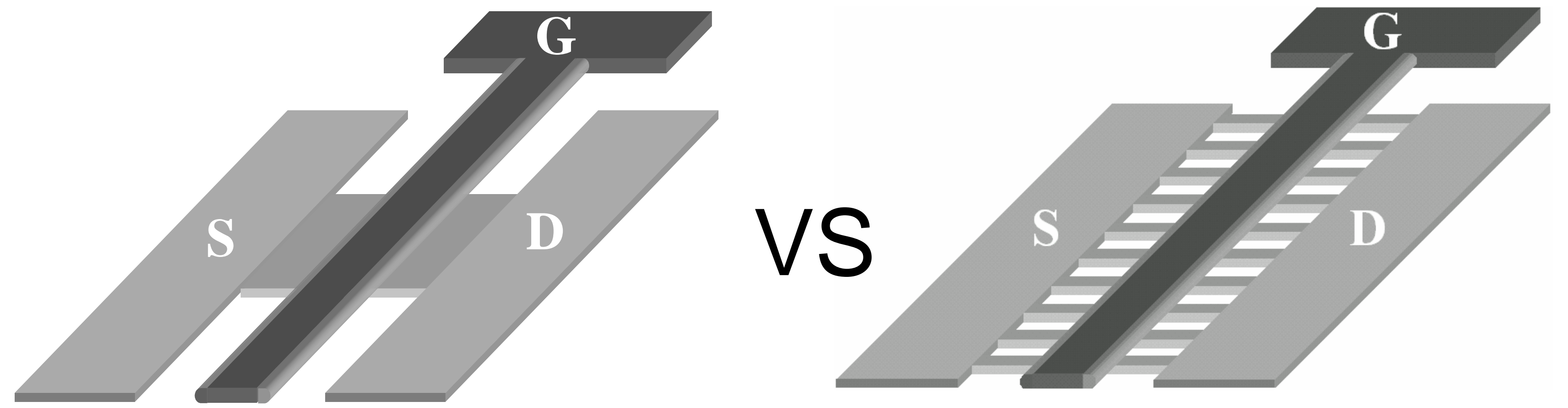


2. Device fabrication



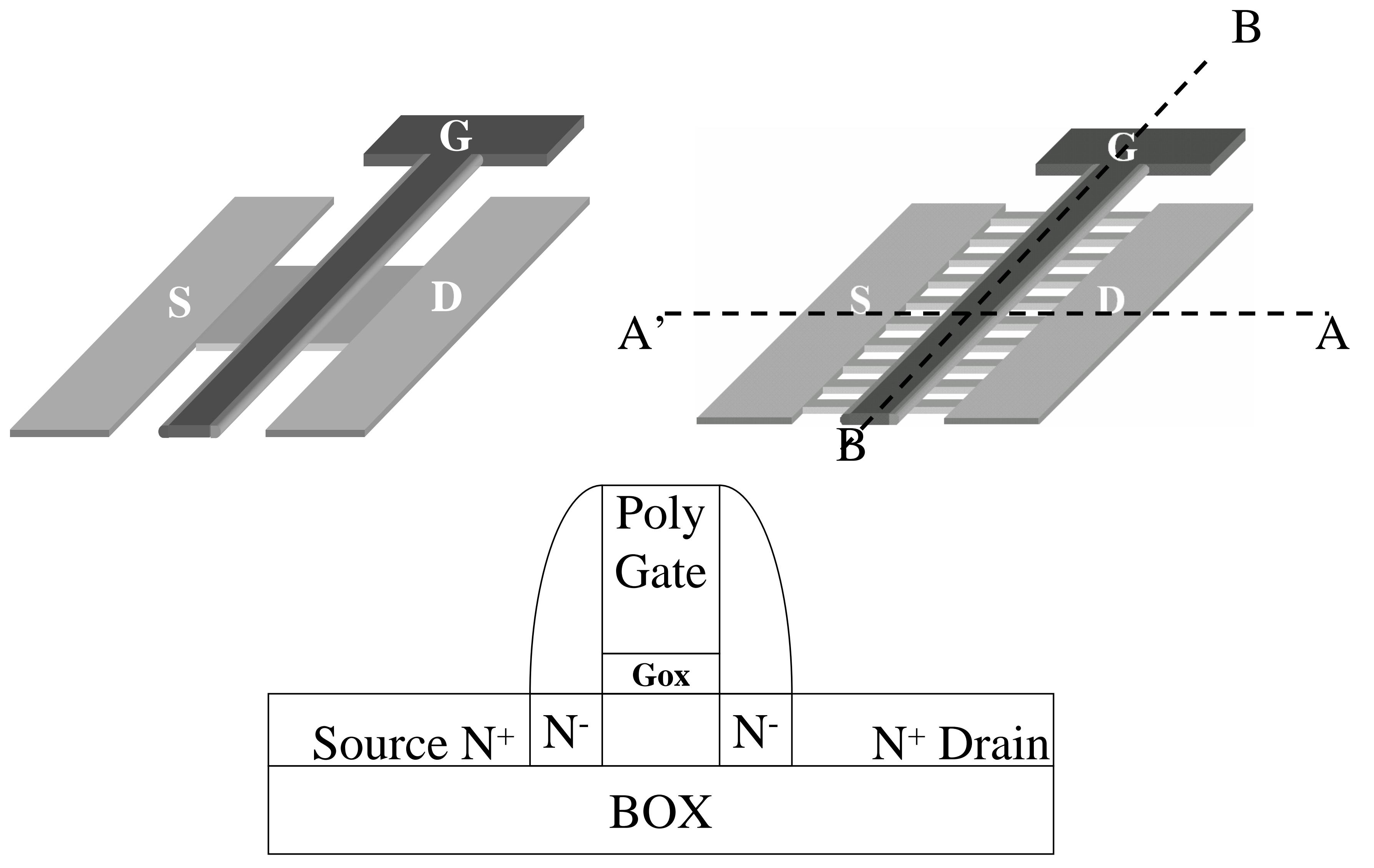
Fabrication steps

1. Buried oxide (400nm) grown
2. 50nm a-Si thin film deposition.
3. SPC crystallization 600^0c 24hr
4. Active region definition
5. Gate definition.
6. N- (5E13)and N+(5E15) implantation & RTA
7. Contact hole and metallization
8. NH3 plasma passivation.



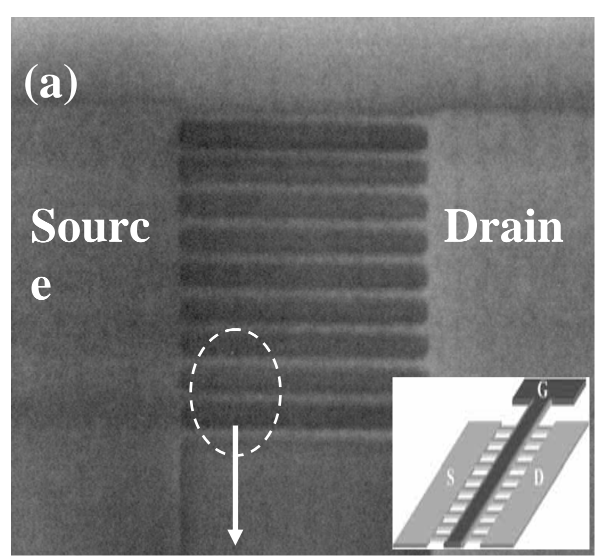
- 3-dimensional schematic plot of purposed conventional single channel TFT.

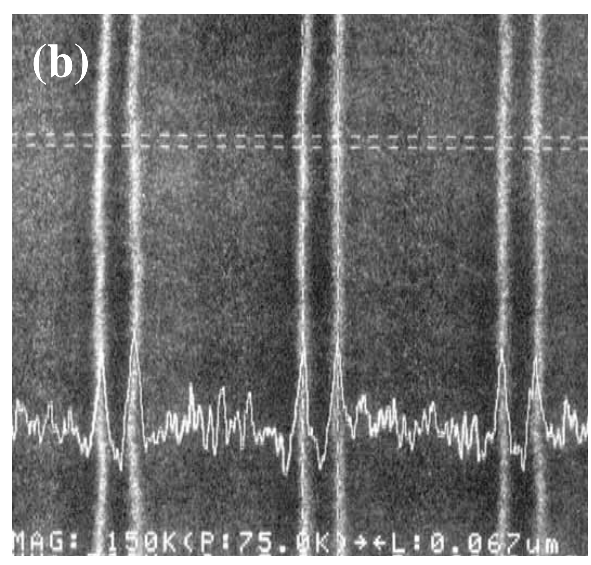
- 3-dimensional schematic plot of purposed multiple nano-wire channels TFT.



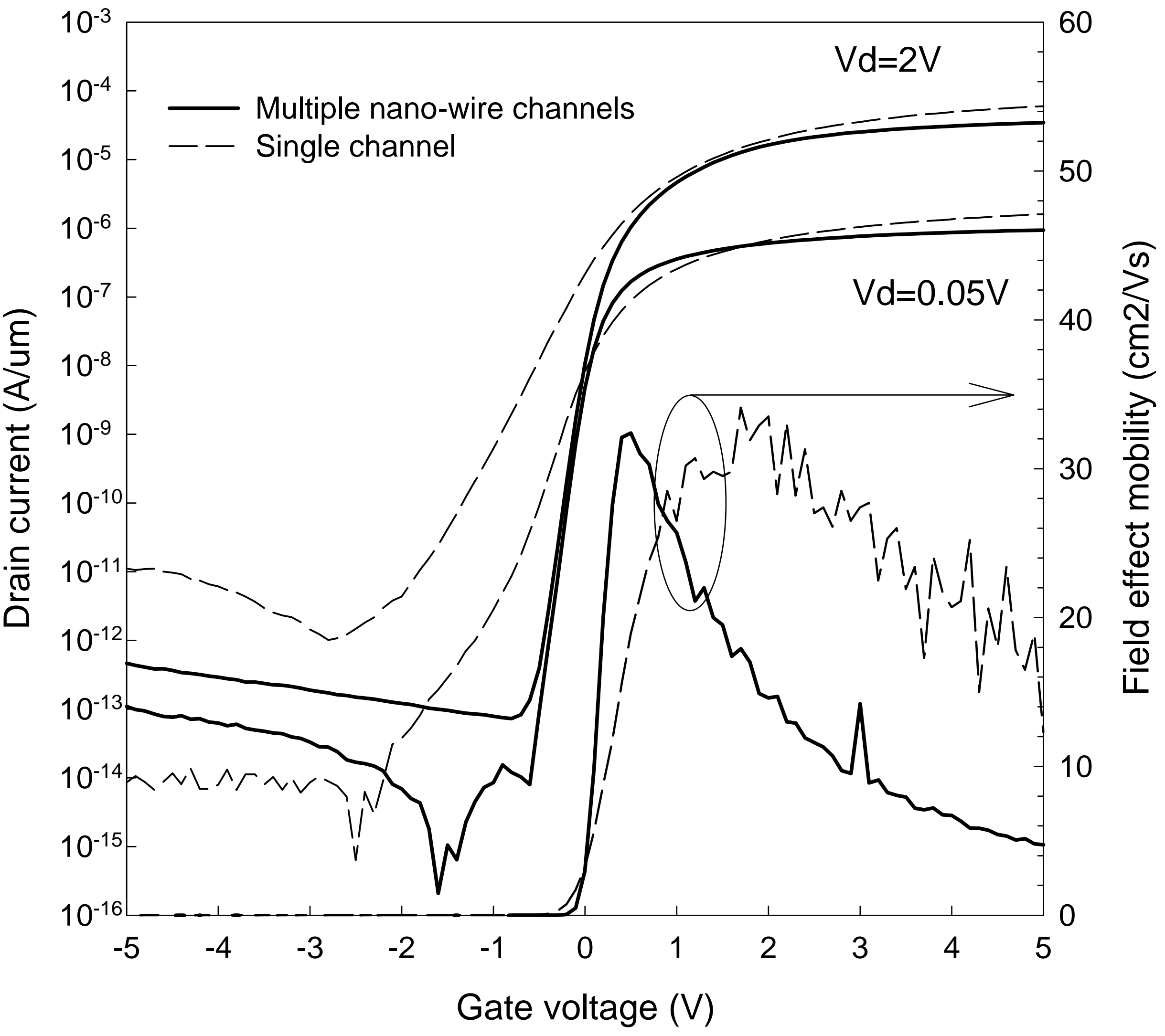
- AA’ Cross-section plot of purposed TFT.

High performance Polycrystalline Silicon TFT with Multiple Nano-Wire Channels

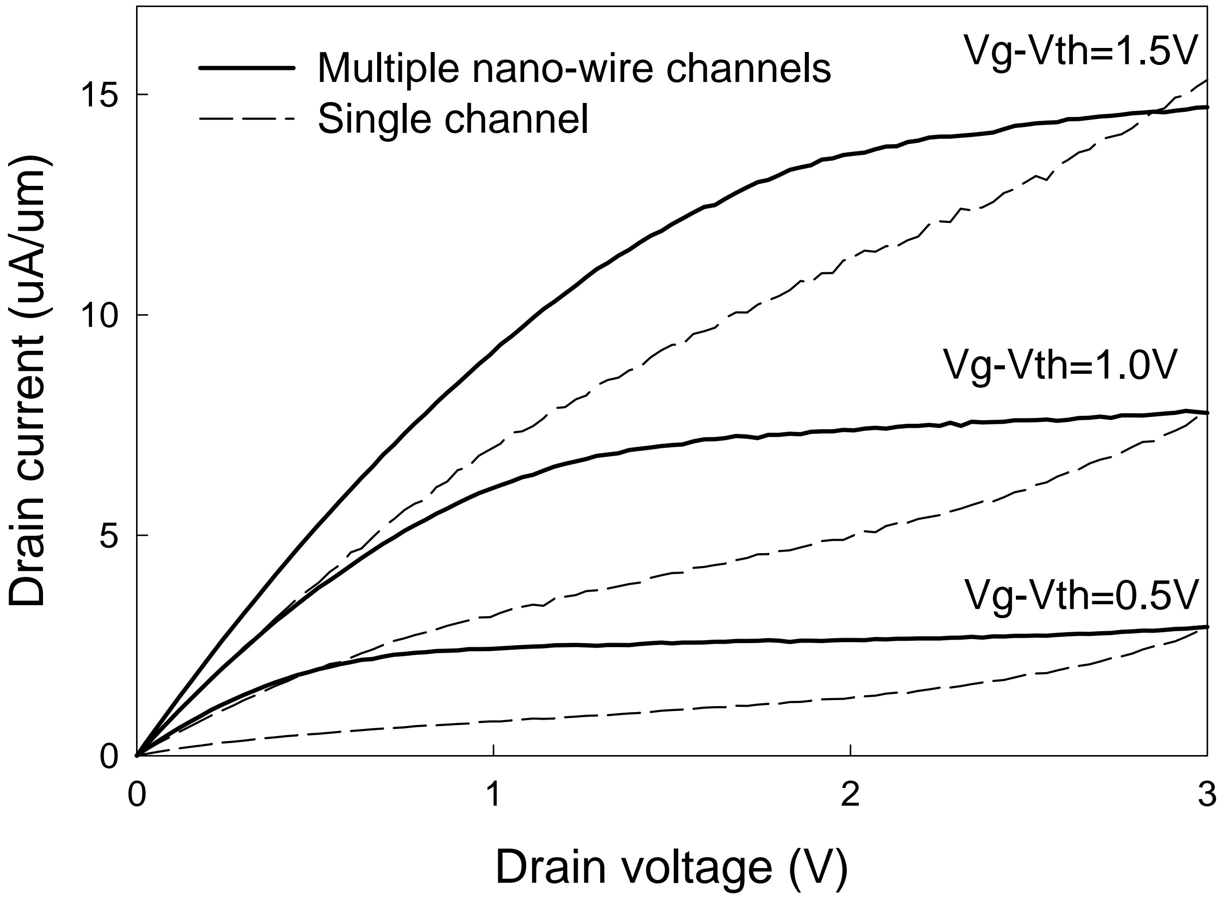




SEM of active pattern with source, drain and multiple nano-wire channels. The each nano-wire width is 67 nm



Id-Vg transfer characteristics of multiple nano-wire channels (L/W = 0.5um/67nm☓10) and single channel (L/W = 0.5um/1um)



"High performance polycrystalline silicon thin film transistor with multiple nano-wire channels and LDD structure"
Applied Physics Letter, 84(19), p.3822 (2004)

Thank you!